

The FPSS L2 Chip

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1. The Algorithm

There are four FPSS cards that process half (East/West) the information from each (North/South) FPS detector. The function of the FPSS L2 chip is to collect all L2 event streams from the eight DFEF boards into one event stream, which is then transmitted via G-link to the L2 FPSS preprocessor. Since the protocols specify at most 48 cluster objects can be transmitted to L2, and it is possible to receive a maximum of 24 clusters from each link, truncation may be necessary. The concatenation of input links happens in three stages. The first stage combines cluster frames from links: 0+1, 2+3, 4+5, and 6+7. The output of the first stage has the same format as the input, so the same functional module is used in the second and third stages where the outputs are pseudo links: (0+1)+(2+3), (4+5)+(6+7). The final stage pseudo link is ordered with low numbered links first: $[(0+1)+(2+3)] + [(4+5)+(6+7)]$. Truncation may happen at the input to each stage. The default scheme is to limit each link to a maximum of six clusters, which allows a maximum of $6 \times 8 = 48$ output clusters. The output of each stage is currently hard-wired to 48 clusters, but can be easily modified. This scheme is symmetric across all links because it will deplete the population of all input links. Other schemes are possible to implement by changing the maximum number of objects stored at each stage; however, the maximum number of objects that can be stored at each successive stage is limited to 30 by the depth of the FIFO used in the design.

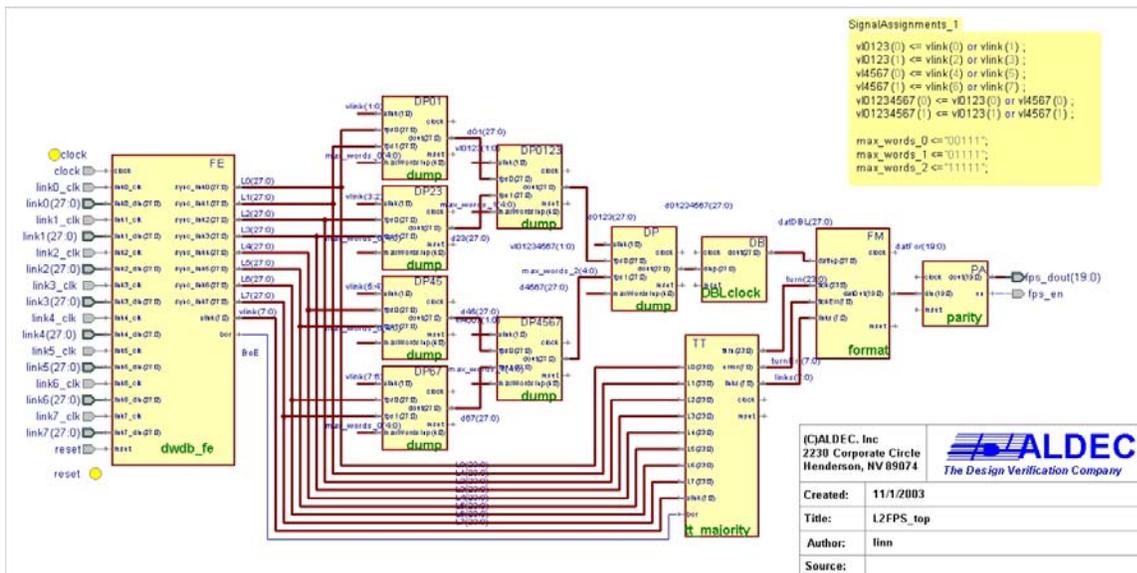


Figure 1 - Block diagram of the FPSS L2 chip.

2. The Design

The top-level block diagram is shown in Figure 1, where the data flows from left to right. First, the inputs links are synchronized to the board global clock by *dwdb_fe*. Then the six instantiations of *dump* execute the concatenation and truncation. This is followed by *DBL_clock*, which stretches the data frames to two clock tics in preparation for the G-link protocol with two frames per cluster. The process *format* generates the G-link formatted data, header, and trailer frames. Finally, the block called parity inserts the vertical parity and pad frames. The block called *tt_majority* accepts the crossing and turn from each input link and outputs single values using a majority vote. The mapping between LVDS input protocol and G-link output protocols is specified in the protocol document and reproduced in Table 1.

Output Frame	Glink Output Bits	Data Field	LVDS Input Bits
1	3-0	0000	
1	4	UV	12
1	7-5	ERROR CODE	
1	14-8	MIP BIT PATTERN	6-0
1	15	MIP	7
2	3-0	TS FPS	11-8
2	4	NS	15-13
2	7-5	PSC WIDTH	23-16
2	15-8	RA PSC FPS	

Table 1. Input/Output mapping

The sixth G-link header frame is used for error reporting. Bits 7-0 when set indicate a missing link on input, and bits 15-8 indicate a crossing/turn discrepancy with the majority vote. Each output cluster has bits 7-5 reserved for error reporting. At this time bit 5 indicates a parity error was discovered on input.

3. The Implementation

The design is implemented on the U3 (D0) chip, and will run at a maximum clock speed of 71 MHz. The L2 output is configured on the so-called *quad_out* or top G-link. Table 2 shows the geometric region covered by each FPSS card and link. There are no controls or monitoring features implemented at this time.

Where	Card	N/S Quadrant	Phi Wedge	LVDS Links
PC20 Crate 2 slot 10	FPSS0	NE	1-8	0-7
PC20 Crate 2 slot 11	FPSS1	NW	9-16	0-7
PC20 Crate 2 slot 12	FPSS2	SE	1-8	0-7
PC20 Crate 2 slot 13	FPSS3	SW	9-16	0-7
PC20 Crate 2 slot 14	FPTT			

Table 2 – Geometric mapping.