

Digital Front End Transition Board

[Rev-2]

Design Report

Engineering Note 2002-10-09a

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29 October 2002

1. General Information

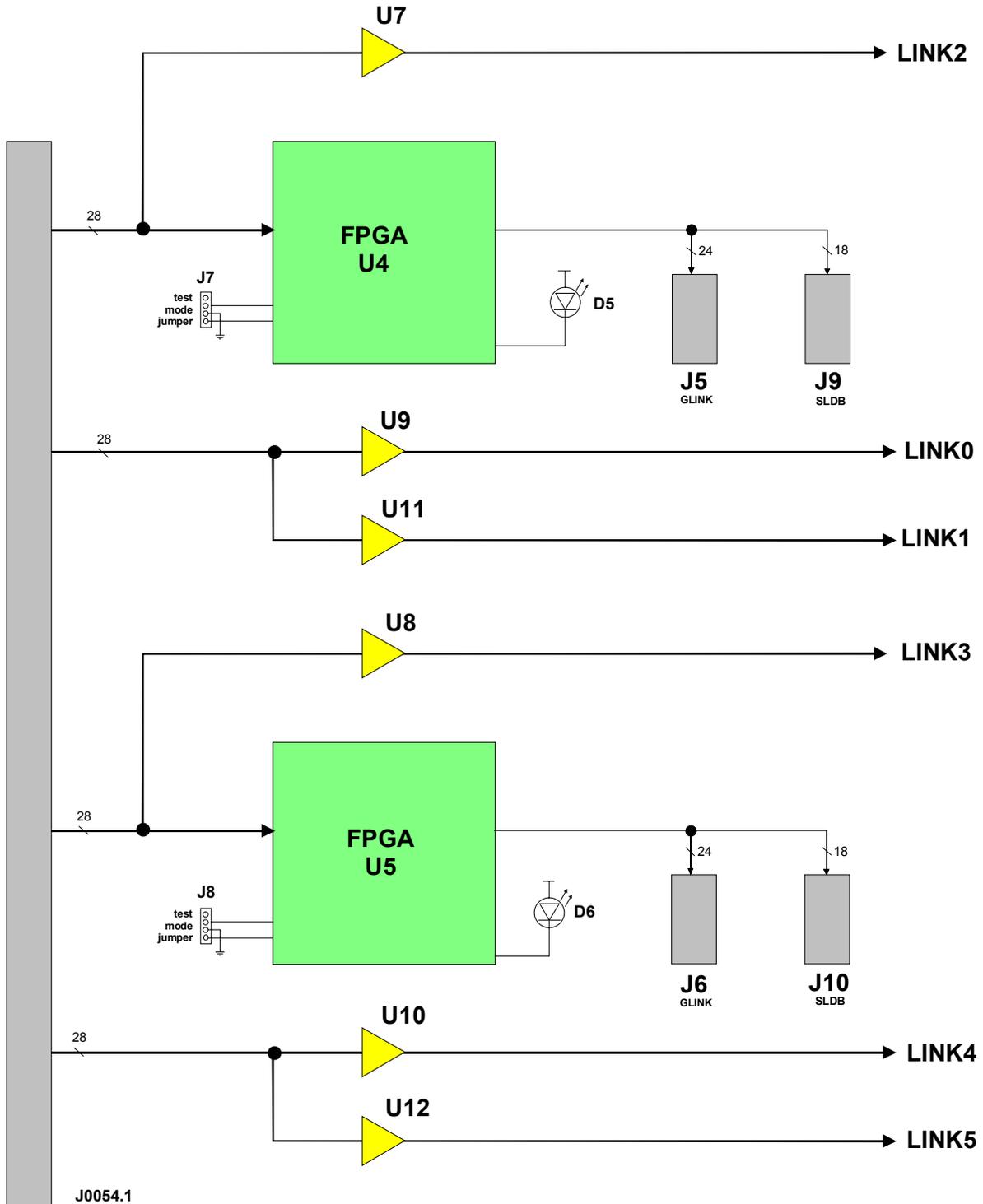
The Digital Front End Transition Board (DFET) is a 6U x 120mm board that is plugged into the backside of a DFE backplane. The DFET receives data, clock, and reset from the DFE motherboard; there are four 28-bit busses supplying the data at 53MHz. Each 28-bit bus goes to at least one LVDS “channel link” transmitter which serializes the data onto four twisted pairs.

Data arriving on two of the four 28-bit busses is sent to either a G-LINK transmitter daughterboard or a serial link daughterboard (SLDB). These two types of daughterboards contain a gigabit-per-second serializer chip that is very sensitive to clock jitter. The clock supplied by the DFE motherboard is too jittery to drive the serializer chips reliably, so an external 53.104MHz crystal oscillator (XTAL) is used to drive those daughterboards. To cleanly transfer data from the DFE motherboard clock to the XTAL clock a dual-port memory and some extra logic is required; the dual-port ram and associated logic is contained in a small FPGA.

The FPGAs also have circuitry built-in to assist with board testing. When plugged into a special test fixture the FPGAs can drive a pattern out on all of the LVDS transmitters. Additionally, the FPGAs test the datapath to the G-LINK / SLDB daughterboard connectors. In this manner all datapaths can be checked out on the bench before installation.

The FPGAs are static-ram based devices, and thus lose their configuration data when power is cycled. A small non-volatile EEPROM is used to store the firmware for each FPGA. Upon power-up the EEPROM automatically loads both FPGAs. The EEPROM can be programmed on the board using the Xilinx JTAG programmer.

2. Dataflow Diagram



3. Firmware

The firmware that resides in the FPGAs has two functions: **normal operation**, where data is buffered in the dual-port ram; and **test modes A and B** and facilitate board-level testing.

1) Normal Operation

DFE Motherboard to G-LINK interface

The G-LINK datapath is 20-bits (plus four control bits). To simplify things for the DFE motherboard firmware designers the FPGA input bus is very simple: the G-link 20-bit data bus maps into the lower 20-bits of the 28-bit bus, plus there is only one control signal, ENABLE, mapped into bit 20:

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							EN	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19

NOTE the G-LINK data bus inversion!

The G-LINK MSb is on the output bus LSB! (Just like the old transition boards.)

When the user wants to send data to the G-LINK, simply set ENABLE. The DFET firmware will handle all of the G-LINK control signals and send the proper fill and data frames. Data must be transmitted in contiguous blocks of no fewer than 12 frames and no more than a few thousand frames long. In between blocks of data ENABLE must be dropped.

DFE Motherboard to SLDB Interface

The SLDB datapath is 16-bits, plus two control signals Transmit Enable (XE) and Parity Enable (PE). Both are active high. These bits are mapped into the DFE-T 28-bit input bus as follows:

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							EN			PE	XE	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

When sending data to the SLDB, **make sure that EN is set whenever XE is set**. Data must be transmitted in contiguous blocks of no fewer than 12 frames and no more than a few thousand frames long. In between blocks of data EN/XE must be dropped. For example, drop EN/XE during the Sync Gap (this is L1muon protocol anyway).

NOTE: In normal operation LEDs D5 and D6 will blink alternately at ~1Hz.

FIFO Buffer Design

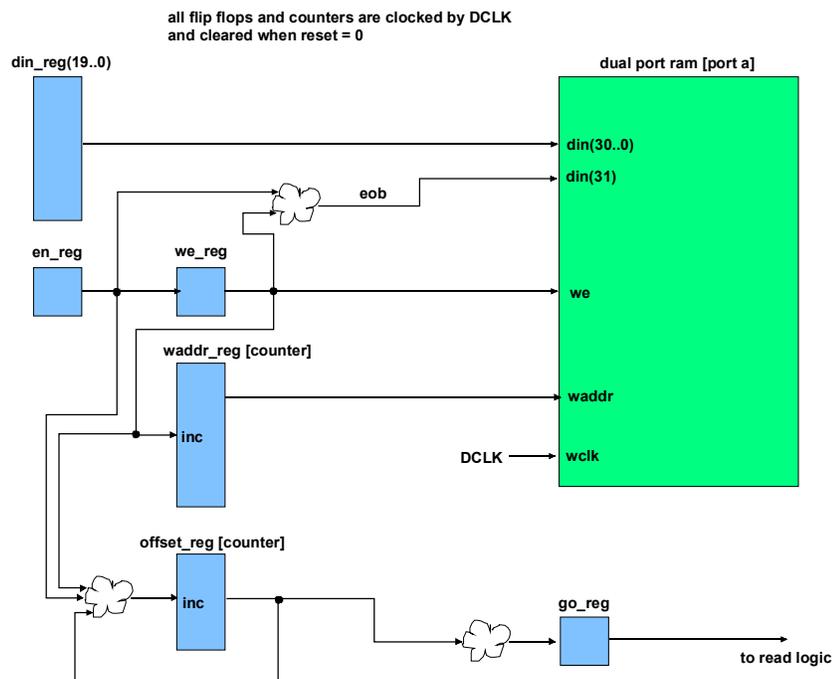
Data is clocked into the FPGA using the DFE motherboard clock (DCLK) and pulled out of the FPGA using the crystal oscillator clock (XCLK). The data must reliably cross from the DCLK domain to the XCLK domain without getting corrupted or truncated.

No assumptions can be made about the relative phases of the clocks. While both clocks are running at ~53.104MHz one must assume that one clock may be slightly faster or slower than the other clock. For example, if the DCLK period is 18.8ps shorter than XCLK then after 1000 clock ticks DCLK will get have supplied one extra clock tick – now the buffer is slowly filling up!

One way to reliably cross a clock domain boundary is to use a dual port ram. Xilinx FPGAs have many true synchronous dual port rams built in. Two of these blockrams are used to make a 32x256 dual port memory. Data is clocked into the ram using DCLK and read out using XCLK. This is basically an asynchronous FIFO operation.

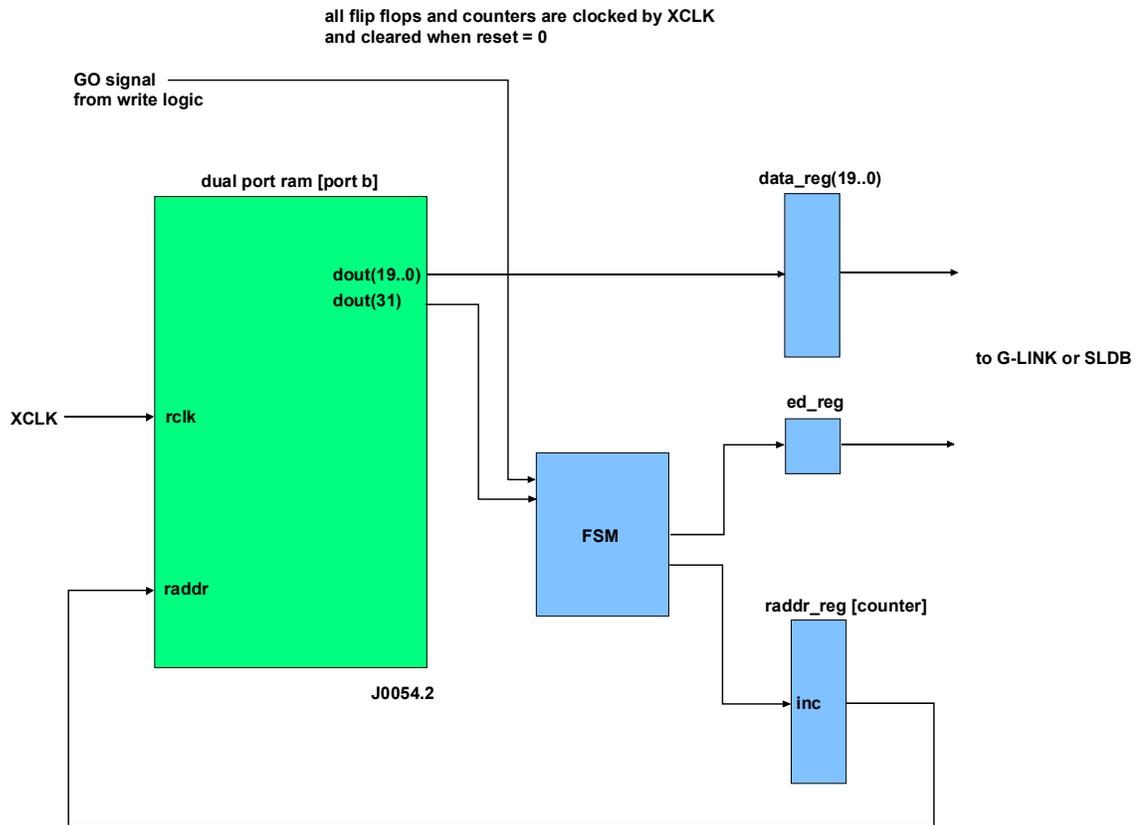
Care must be taken to offset the read and write pointers so that the FIFO doesn't gradually fill up or empty out because the clock frequencies differ slightly. When the write logic sees ENABLE go high it immediately begins to write the data into the dual port ram. After 12 writes it sends a signal (GO) to the read logic telling it to begin reading from the ram. When the write logic detects the end of the data block it sets the bit 31 of the last word it clocks into the ram. This bit tells the read logic to stop reading. Since the GO signal originates in the DCLK domain but is sampled in the XCLK domain, it is asserted for two DCLK cycles, guaranteeing it will be sampled by XCLK.

Write Logic (DCLK domain; file front_end.vhd)



Offset_reg is reset to 0 when the beginning of block is detected, otherwise it counts up to 15 and halts. When the count is equal to 12 or 13, go_reg is set. This allows the FIFO to fill up with about 12 frames before the read logic is told to start reading. EOB is set to mark the last frame of the block – when the read logic reads this frame from the ram it will stop and wait for a new GO signal.

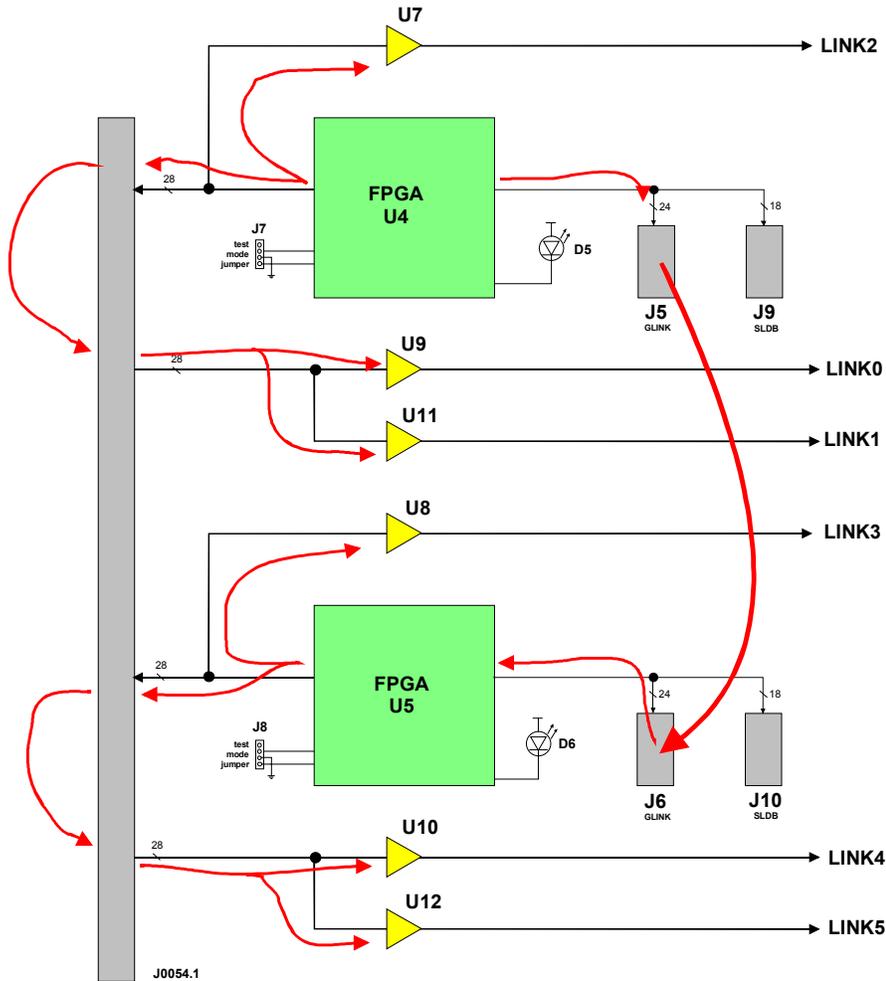
Read Logic (XCLK domain, file back_end.vhd)



The read logic has a very simple state machine. When IDLE, ed_reg is zero and the read pointer (raddr_reg) is not incrementing. When the GO signal is seen the state transitions to START and then READ and the read pointer increments and ed_reg is set. The state machine stays in READ until it sees dout(31) set, then it transitions back to IDLE. Ed_reg drives the G-LINK control signal ED (enable data). The three other G-Link control signals are static: DAV=1, CAV=0, and FF=1.

2) Test Mode A

In this test mode the FIFOs are disabled. Each FPGA input bus becomes a 28-bit output bus driving a walking-ones pattern. When the DFET is connected to the test fixture, the johnson counter pattern is driven off the board and back on to drive the two LVDS transmitters as shown below:



Device U4 also drives out a 24-bit johnson counter pattern on its output bus. A small PCB board is connected to the DFE-T that connects J5 and J6 together. Then device U5 checks for the johnson counter pattern. If the pattern is error free U5 lights LED D6. If there is an error in the pattern D6 turns off for ~0.25 seconds.

3) Test Mode B

This test mode works very much like test mode A except that the johnson counter pattern driven by U4 is only 18 bits, and a different PCB is used to connect J9 and J10 together. Device U5 checks the 18-bit pattern for errors and lights D6 if everything is OK.

A datapump can be connected to the LVDS outputs (LINK0~LINK5) and manually checked for the presence of the walking-ones pattern.

4) Simulation and Implementation

Functionally simulated in Aldec Active-HDL 5.2. After synthesis and place and route in a Xilinx Spartan II device the maximum clock rate is ~100MHz. Minimum setup time needed on the inputs is ~3ns, and the clock to Q time on the outputs is ~7ns. Device utilization is about 50% for U4 and about 80% for U5 (it has more checking to do in the test modes).

The two FPGA bitfiles were concatenated into a single EEPROM image file called **trans_v10.mcs**

4. References

Xilinx Spartan II datasheets

www.xilinx.com

Xilinx XAPP130: Using the Virtex Block SelectRAM+ Features

www.xilinx.com/xapp/xapp130.pdf

Xilinx XAPP138: Virtex FPGA Series Configuration and Readback

www.xilinx.com/xapp/xapp138.pdf

Xilinx XAPP132: Using the Virtex Delay-Locked Loop

www.xilinx.com/xapp/xapp132.pdf

5. Revision History

29 October 2002: G-LINK data bus direction swap added to section 3.1