

# DFEF

## **Technical Design Report**

**ver 1.00**

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**DØ Experiment**

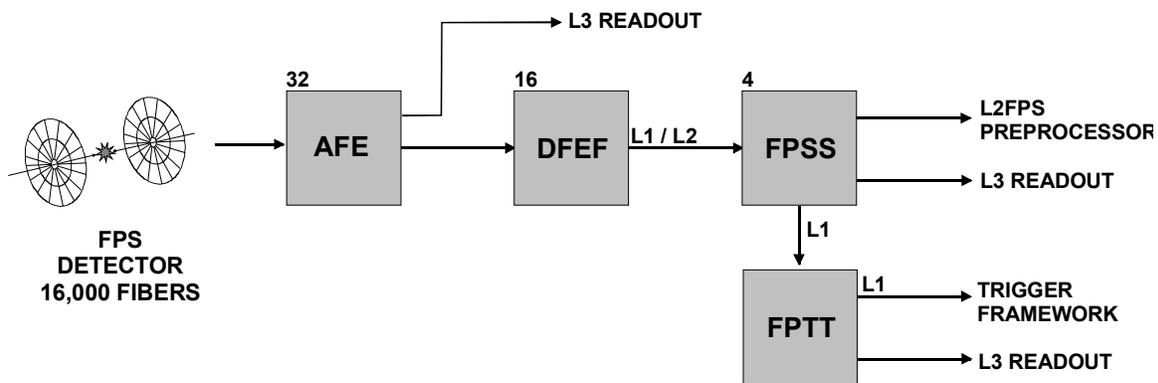
**Fermi National Accelerator Laboratory**

# 1. INTRODUCTION

The DFEF, FPSS, and FPTT boards are responsible for forming L1 trigger bits from the Forward Pre-Shower detector, one of three sub-detector which form the Central Track Trigger (CTT) [1]. The DFEF board is the first level board in the Forward Pre-Shower (FPS) system; it is responsible for unpacking fiber discriminator bits from the Analog Front End (AFE) boards and finding clusters in an FPS “wedge”. There are 16 North and 16 South wedges in the FPS system; each wedge contains four layers: U and V shower (144 strips each) and U and V mip (103 strips each).

The DFEF finds clusters and checks strips in the MIP layer to see if there is match. Clusters and their associated MIP information are counted for L1 but stored for later L2 readout.

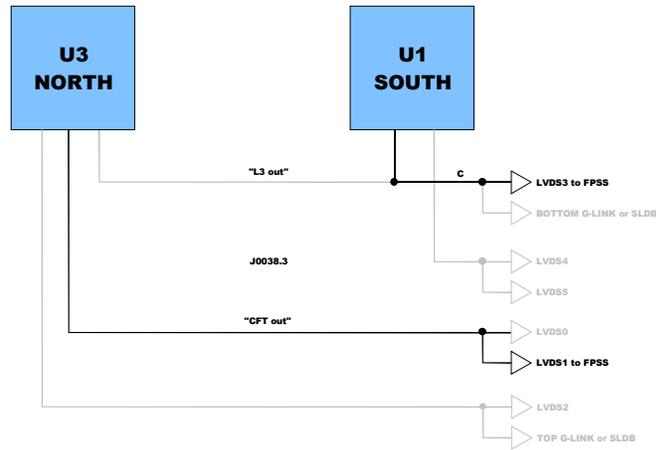
# 2. FPS CHAIN DIAGRAM



The 16 DFEF boards each receive eight 21-bit LVDS cables from the AFEs. Each DFEF board handles two wedges, one North and one South. There are two 28-bit LVDS output links driven by each DFEF board; each LVDS link sends L1 and L2 records to the FPSS boards.

### 3. DFEF BUS STRUCTURE

Each DFEF board contains two FPGAs. Each FPGA is an Virtex 1000E device. Two wedges are handled by one DFEF board. Device 0 (U3) always handles a NORTH wedge; Device 2 (U1) always handles a SOUTH wedge.



Ten 28-bit LVDS inputs feed into both FPGAs on the DFEF board, however, only busses 0-7 are used. The north wedge sends out the L1/L2 records on the "cft out" bus; the south wedge sends its L1/L2 records out on the "L3 out" bus. Currently each DFEF board has two LVDS outputs only; no GLINKs or SLDBs are used. (However, U3 could be used to drive a GLINK transmitter to L3 if need be.)

*Device U3 should not drive the "L3 out" bus otherwise bus contention will occur, damaging the FPGAs.*

### 4. RECORD TYPES AND DEFINITIONS

#### 4.1. INPUT RECORDS

The AFE boards generate 7 frame L1 records continuously. The least significant bit is used as a SYNC marker (not to be confused with the SYNC\_GAP control bit) which is set to mark the last frame of the record. Since each of the 128 LVDS links is different, a database is used to keep track of the discriminator bits. The complete mapping is available at the DFE documentation connections page [2].

System control bits are embedded in the last frame of the input records. They are:

- **S** Sync marker – marks the last frame of the record
- **FX** First Crossing -- marks crossing number 7
- **CR** CFT\_Reset (same as SCL INIT)
- **SG** Sync Gap -- marks the sync gap (not the cosmic gap)
- **L1** L1 Accept (also called L1a, L1acc)
- **BM** Beam 396

## 4.2. OUTPUT RECORDS

DFEF L1 and L2 records follow the format specified in the *Protocols Document*. [3]

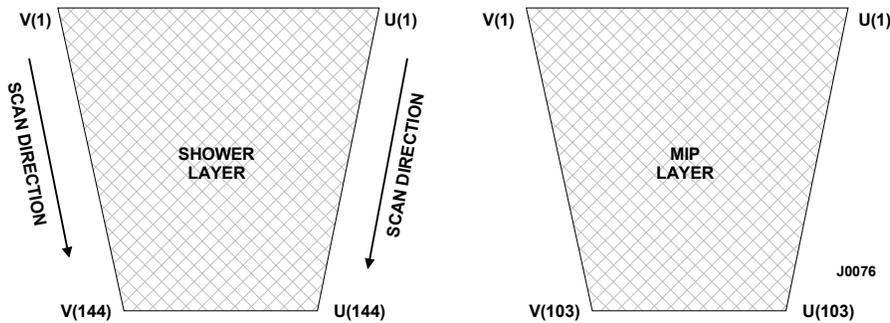
For L1 records, the U cluster counts are sent first, in timeslice 2, followed by the V cluster counts. For both cases the MIP / No MIP counts are exclusive. The [TS FPS] field encodes the wedge number from 1 (0000) to 16 (1111); the North and South bits describe which end cap the wedge is associated with. The East bit is set for wedge numbers 1-8; the West bit set for wedges 9-16. Pass-N-Mark [P/M] bits are always set to 00.

The L2 record is a “dummy” record containing no cluster information (#obj = 0). However, the tick and turn numbers are real. The [N/S] bit is set for North wedges, and the [E/W] bit is set for wedges 1-8. Pass-N-Mark [P/M] bits are always set to 00. The purpose of this “dummy” L2 record is to alert the FPSS board that a L1 accept occurred.

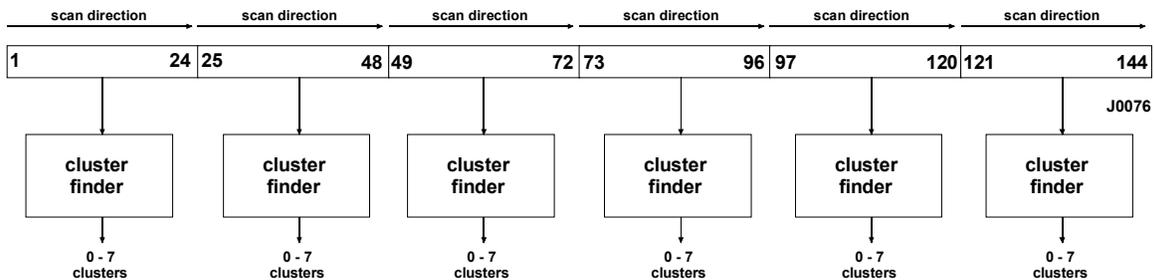
## 5. DFEF FUNCTIONS

### 5.1.1. FINDING CLUSTERS

The DFEF finds clusters in the shower layer, which consists of 144 U strips and 144 V strips.



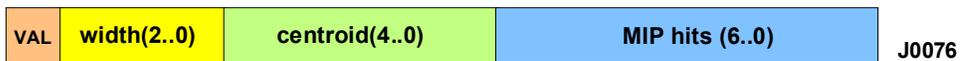
U and V strips are processed independently; no cross checking or other information sharing occurs between U and V cluster finder circuitry. Each 144-bit array is broken into six 24-bit sections, and each of these sections is fed into a cluster finder module. Each cluster finder module starts with the low numbered strip and scans across the strips, reporting the first seven clusters it finds. Clusters are described in terms of centroid and width. *Note that a cluster which spans the boundary between two 24-bit sections will be reported as TWO smaller clusters. No effort is made to combine these smaller clusters back into a single, larger cluster.*



### 5.1.2. CLUSTER MATCHING

When a cluster is found in the shower layer, corresponding strips are checked in the MIP layer; if there are any hits in these MIP strips the shower cluster is considered to have a MIP match. For example, a U cluster is found with a centroid equal to 53. Next, U layer MIP strips [53..47] are checked to see if there are any hits; if any of these seven MIP bits are set, the DFEF considers this cluster to have a MIP layer match. Again, U and V cluster logic is treated separately, even during MIP matching no U and V information is shared.

The MIP layer hits become part of the internal cluster format:



Where VAL is set for valid clusters. The cluster width goes from zero (really means zero) to seven; clusters wider than 7 strips are reported as having a width of seven. The centroid goes from 1 to 24; to know the absolute cluster centroid one must know which cluster finder module found the cluster. The MIP layer bits are the raw discriminator bits from the MIP layer.

Note that the cluster width is NOT taken into account when checking for a MIP layer match. MIP strips are selected solely based on the centroid of the shower layer cluster.

### 5.1.3. FORMING L1 COUNTS

A cluster is considered matched if there are one or more set bits in the associated MIP layer strips.

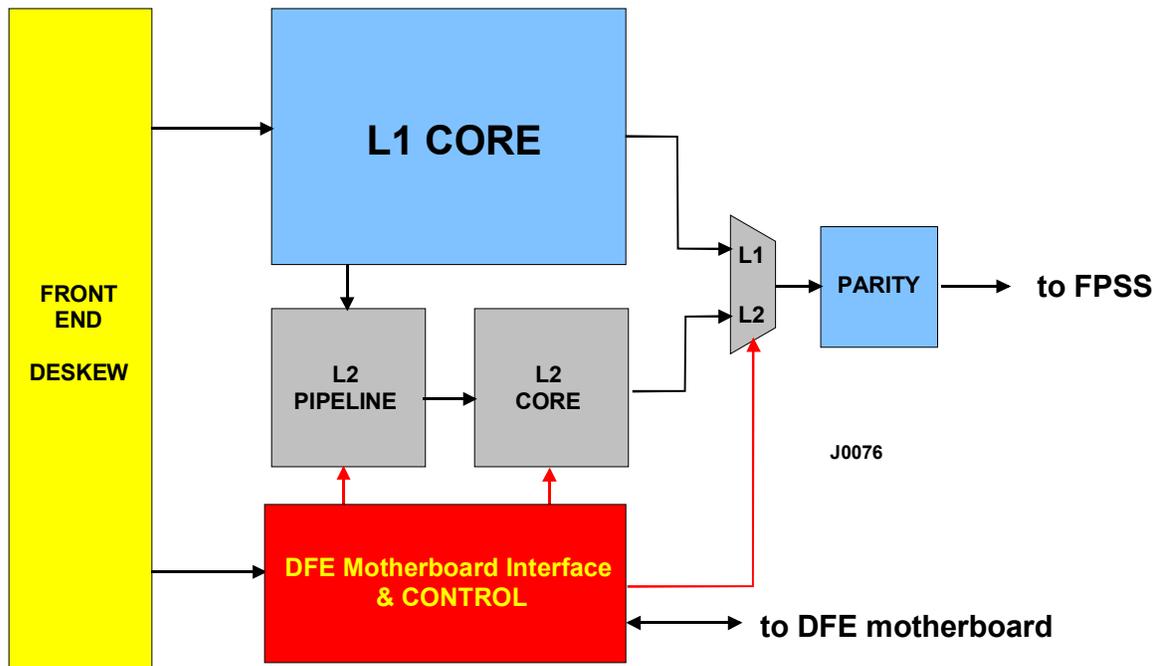
### 5.1.4. STORING CLUSTERS FOR L2 READOUT

Raw cluster information is stored in pipeline for later readout if a L1accept should occur. The depth of the pipeline is from 0 to 64 132ns crossings deep, and this depth is dynamically adjustable. There are 6U and 6V cluster busses in the DFEF; each bus is time multiplexed, transferring 7 clusters per crossing. A total of  $12 \times 7 = 84$  clusters are stored in the pipeline each crossing for L2 readout.

### 5.1.5. SORTING AND REPORTING CLUSTERS FOR L2

When a L1accept occurs the DFEF looks back in the pipeline and fetches the raw clusters for the target event. A maximum of 24 clusters are reported in the L2 record: 0 to 12 U clusters followed by 0 to 12 V clusters. Clusters are sorted in order of decreasing eta (increasing centroid strip number). *This algorithm has not been implemented yet.*

## 6. DFEF BLOCK DIAGRAM



### 6.1. FRONT END

The front end deskews the eight LVDS input links, moving them over into the global clock domain. The front end is also responsible for checking the status of the input links, and it produces three types of diagnostic bits:

- **Valid Link.** The front end checks that each input link receives an *End of Record* (EoR) marker periodically. If an EoR marker is not seen within 32 clock cycles, the DFEF marks this input as missing.
- **EOR Error.** The AFE boards must send an EoR marker one out of every 7 clock cycles. If this fails to occur, the front end sets the corresponding bit in this array. Basically a more stringent version of valid link.
- **Sync Error.** After deskewing the input links the front end checks that all input links' EoR markers are asserted in the same clock cycle.
- **Pattern Error.** The front end can detect the presence of the AFE "walking 1's" test pattern. If this pattern is present end error free, the front end will clear the corresponding bit in this array. Used only for AFE-to-DFEF link tests, not in normal running.

Additionally, the front end strips off the control bits (BoR, FX, CR, L1a) and aligns them with the synchronized link data presented to the L1 core.

The front end also calculates the tick and turn number. The circuitry that calculates the tick and turn number is constantly monitoring the FX and CR control bits. If these control bits show up at the expected time, the tick and turn counter asserts the LOCKED status bit. However, the counters are capable of "riding through" a missed FX control bit without dropping the LOCKED bit -- if this occurs, the *bad\_fx* status bit is pulsed momentarily. Once LOCKED is dropped the tick and turn counters are cleared until a CR (aka SCL init) occurs. Hard resetting a DFEF board will cause it to drop LOCKED as well.

## 6.2. L1 CORE

This module is responsible for finding U and V clusters, associating the clusters with MIP layer hits, and counting the number of clusters with and without a MIP match. The L1 core module continuously outputs L1 records, which get passed along to the FPSS.

The L1 core can also generate fake L1 records which are used for diagnostics and troubleshooting. See appendix XXX for details on these modes.

Raw clusters found in the L1 core are passed on to the L2 Pipeline module to be stored for later readout.

## 6.3. L2 PIPELINE

Up to 42 U and 42 V clusters are stored in this memory. It's constructed from BlockRAM primitives, and the depth is dynamically adjustable from 0 to 64 [132ns] crossings deep. The tick and turn numbers are also stored in the pipeline, as this insures that the RAW clusters are closely associated with the tick and turn numbers and eliminates errors that might be caused by recalculating the tick and turn number later during L2 readout.

The pipeline always runs in this design. As one set of clusters enters the pipeline, an old set of clusters falls out the other end.

## 6.4. L2 CORE

When a L1accept occurs, the L2 core “catches” the raw clusters as they fall out of the end of the L2 pipeline. The clusters are then sorted and truncated (12 U and 12 V clusters). This list of clusters is wrapped in a L2 record and transmitted to the FPSS.

The L2 core can also generate fake L2 records for troubleshooting.

## 6.5. PARITY

This module adds horizontal and vertical parity to L1 and L2 records. *Note that this module goes not correct the horizontal and vertical parity fields for the [number of objects] field in the L2 record header.*

A mux in front of this module selects which core gets to send its record to the FPSS. The switchover must happen cleanly, at record boundaries, otherwise the parity module will get confused and garble the output.

## 6.6. DFE MOTHERBOARD INTERFACE & CONTROL

There are really two separate functions contained in this block: Control and Interface.

### 6.6.1. DFEF CONTROL

This module is designed to sequence the cores and pipelines based on state machines controlled by control bits (FX, CR, L1a, etc.). For example, the control logic tells the L2 core when to begin grabbing the raw clusters falling out of the L2 pipeline; it tells the parity mux when to switch over from L1 records to L2 records, etc. The control logic is the “brain” of the DFEF, it is intimately aware of the latency and operation of each module in the design; it facilitates the movement of data through the various pipelines.

### 6.6.2. DFE MOTHERBOARD INTERFACE

In contrast to the fast control logic, the motherboard interface functionality is very slow. This module talks to the online computers via the DFE motherboard, DFE backplane, and DFE crate controller (DFEC) and the 1553 network. Some examples of things that are done over this interface are:

- Setting the L2 pipeline depth
- Reading the front end link diagnostic bits (valid link, EOR error, etc.)
- Reading control bit diagnostics (LOCKED, bad\_fx, etc.)
- Setting L1 and L2 fake record modes

Status information is sent out one byte at a time. Since there are more than 8 status bits in the DFEF, they are divided into single byte “pages” which are selected one at a time. This interface supports 16 status pages, listed below:

| page | s7                | s6         | s5         | s4         | s3           | s2         | s1         | s0         |
|------|-------------------|------------|------------|------------|--------------|------------|------------|------------|
| 0    | FXX               | BMFX       | L1X        | L1A        |              | ML         | SE         | LOCK       |
| 1    |                   |            |            | North      | Wedge Number |            |            |            |
| 2    | Output Control    |            |            |            |              |            |            |            |
| 3    | L2 Pipeline Depth |            |            |            |              |            |            |            |
| 4    |                   |            |            |            |              |            |            |            |
| 5    | 0                 | 1          | 0          | 1          | 0            | 1          | 0          | 1          |
| 6    | 1                 | 0          | 1          | 0          | 1            | 0          | 1          | 0          |
| 7    |                   |            |            |            |              |            |            |            |
| 8    |                   |            |            |            |              |            |            |            |
| 9    |                   |            |            |            |              |            |            |            |
| 10   |                   |            |            |            |              |            |            |            |
| 11   |                   |            |            |            |              |            |            |            |
| 12   | Miss-link7        | Miss-link6 | Miss-link5 | Miss-link4 | Miss-link3   | Miss-link2 | Miss-link1 | Miss-link0 |
| 13   | Sync-err7         | Sync-err6  | Sync-err5  | Sync-err4  | Sync-err3    | Sync-err2  | Sync-err1  | Sync-err0  |
| 14   | EOR-err7          | EOR-err6   | EOR-err5   | EOR-err4   | EOR-err3     | EOR-err2   | EOR-err1   | EOR-err0   |
| 15   | Patt-err7         | Patt-err6  | Patt-err5  | Patt-err4  | Patt-err3    | Patt-err2  | Patt-err1  | Patt-err0  |

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Orange cells possess the history property. History bits are checked on every clock tick (53MHz) – if the status bit goes high once, the corresponding history bit will stay high until manually cleared. This enables the interface to catch spurious events such as parity and pattern errors.

- **FXX.** FX Xor. Each input link to the DFEF includes an FX control bit. These bits are XOR’ed together, so if there is any disagreement between these input links the FXX status bit will be set.
- **BMFX.** Bad Master FX. The tick and turn counters look at the control bits embedded in LINK2. Once the tick and turn counters are locked onto the AFE boards they know when to expect the FX bit. If the FX bit arrives at an unexpected time this bit will be set.
- **L1X.** Logical XOR of all L1\_ACCEPT control bits on the input links. If there is a disagreement this bit will be set.

- **L1A.** This bit is set whenever the DFEF sees a L1\_ACCEPT control bit arrive on LINK2.
- **ML.** logical OR of the eight missing link bits in status page 12.
- **SE.** logical OR of the eight sync error bits in status page 13.
- **LOCK.** this bit is set if the tick and turn counters are incrementing normally and are happily locked to the AFE control bits. If this bit goes low an SCL\_INIT will need to be issued by the DAQ system.
- **North.** This bit is set if the DFEF FPGA is associated with North wedge. This is hard-coded in the firmware.
- **Wedge Number[3..0].** Wedges 1 (0000) through 16 (1111) are valid. This is hard-coded in the DFEF firmware.
- **Output Control [5..0].** these 6 bits control what kinds of output records are sent out of the DFEF. See the next section for details.
- **Pipeline Depth [5..0].** these six bits show the depth (in 132ns crossings) of the L2 pipeline.
- **Pages 5 and 6** are static bytes used for debugging the interface.
- **Miss-Link [7..0].** If the DFEF front end doesn't receive an EoR marker on an input link within 32 clock cycles it sets the corresponding bit in this array.
- **Sync-Error [7..0]** All deskewed links' EoR markers are compared against LINK2's EoR marker. If there is any difference the corresponding bit in set in this array.
- **EoR-Error[7..0]** Each input link must see an EoR marker one out of every seven clock ticks, if this is not the case the corresponding bit is set in this array.
- **Patt-Error[7..0]** If the DFEF front end detects an error in the AFE's "walking 1's" test pattern it sets the corresponding bit in this array.

### 6.6.2.1. SETTING PARAMETERS

After the DFEF is initialized, parameters may be written to the two FPGAs on the board. One example would be to change the pipeline depth. Currently four operations are supported: clear history, set status page, set L2 pipeline depth, and set the output control bits.

| 7 | 6 | 5              | 4  | 3           | 2 | 1 | 0 |
|---|---|----------------|----|-------------|---|---|---|
| 0 | 0 |                | CH | Page Select |   |   |   |
| 0 | 1 | L2 Pipe Depth  |    |             |   |   |   |
| 1 | 0 |                |    |             |   |   |   |
| 1 | 1 | Output Control |    |             |   |   |   |

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Some examples. Note, all of these macro fragments assume that we're talking to a DFEF board in slot 12. On all DFEF boards the NORTH wedge is device 0, and the SOUTH wedge is device 2.

```
# set the pipeline depth to 36 for the DFEF U3 FPGA (North Wedge)
# 36 = 0x24; 0x24 or'ed with 0x40 = 0x64
set DFE 12
set device 0
cmd writebyte 3 0x64
```

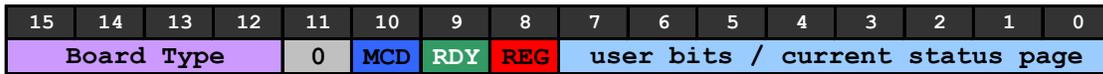
```

# instruct the DFEF south wedge FPGA (U1) to return it's position
# (send back status page1)
set DFE 12
set device 2
cmd writebyte 3 0x01

# clear history and display status page 12
set DFE 12
set device 0
cmd writebyte 0x0c
cmd writebyte 0x1c
cmd writebyte 0x0c

```

### 6.6.2.2. SLOW MONITOR WORD



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All DFEF boards continuously return a 16-bit status word to the crate controller. The most significant nibble is a board type identifier, which is not used anymore. MCD is the master clock detect bit – it's set if the DFEF master clock is >50MHz. RDY is set if both FPGAs have been properly initialized. REG goes LOW if the regulator in the DFEF board is having problems maintaining a stable FPGA core voltage of 1.8V. The lower byte of this word is the status page byte; one of 16 possible status pages is selected by the user (see the previous section).

## 7. DIAGNOSTIC OUTPUTS

These outputs are for the current DFEF build version 000.004, which has a fake L2 core. This version produces real L1 output records, but the L2 outputs are fake, with real tick and turn numbers.

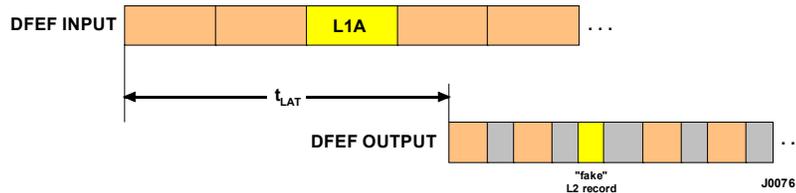
The output control (OC) bits are defined as:

| <u>value</u> | <u>L1 record</u>              | <u>"dummy" L2 record?</u> |
|--------------|-------------------------------|---------------------------|
| 0x00         | normal                        | Y                         |
| 0x01         | normal                        | N                         |
| 0x02         | set all counts to zero        | Y                         |
| 0x03         | all counts to 1               | Y                         |
| 0x04         | all counts to 1 on First Xing | Y                         |
| 0x3E         | L1 link test pattern          | N                         |
| 0x3F         | completely zero the output    | N                         |

## 8. TIMING AND LATENCY

For DFEF build version 000.004 total latency ( $t_{LAT}$ ) is 620.4ns or 33 53MHz clock cycles. Normal DFEF output records are four frames long, including parity. The inter-record gaps are 3 frames long, guaranteed to be zero. The “fake” L2 record is three frames long, including parity, followed by four null frames.

Currently the L1 latency and L2 latency are the same.



## 9. DEVICE RESOURCES

Device utilization summary:

|                               |                   |      |
|-------------------------------|-------------------|------|
| Number of External GCLKIOBs   | 4 out of 4        | 100% |
| Number of External IOBs       | 207 out of 404    | 51%  |
| Number of LOCed External IOBs | 207 out of 207    | 100% |
| Number of SLICES              | 4141 out of 12288 | 33%  |
| Number of GCLKs               | 4 out of 4        | 100% |

## 10. REVISION HISTORY

- 001 3 September 2003: core algorithms only
- 1.00 4 Nov 2003. DFEF firmware version 000.004, with fake L2 core.

## 11. REFERENCES

1. J. Olsen et al., “The DØ Central Track Trigger,” IEEE Trans. Nucl. Sci., submitted for publication.
2. DFE Connection Documentation webpage:  
<http://www-d0online.fnal.gov/www/groups/cft/CTT/online/docs/interconn/connections.html>
3. DFE Protocols Documentation:  
<http://www-d0online.fnal.gov/www/groups/cft/CTT/online/docs>