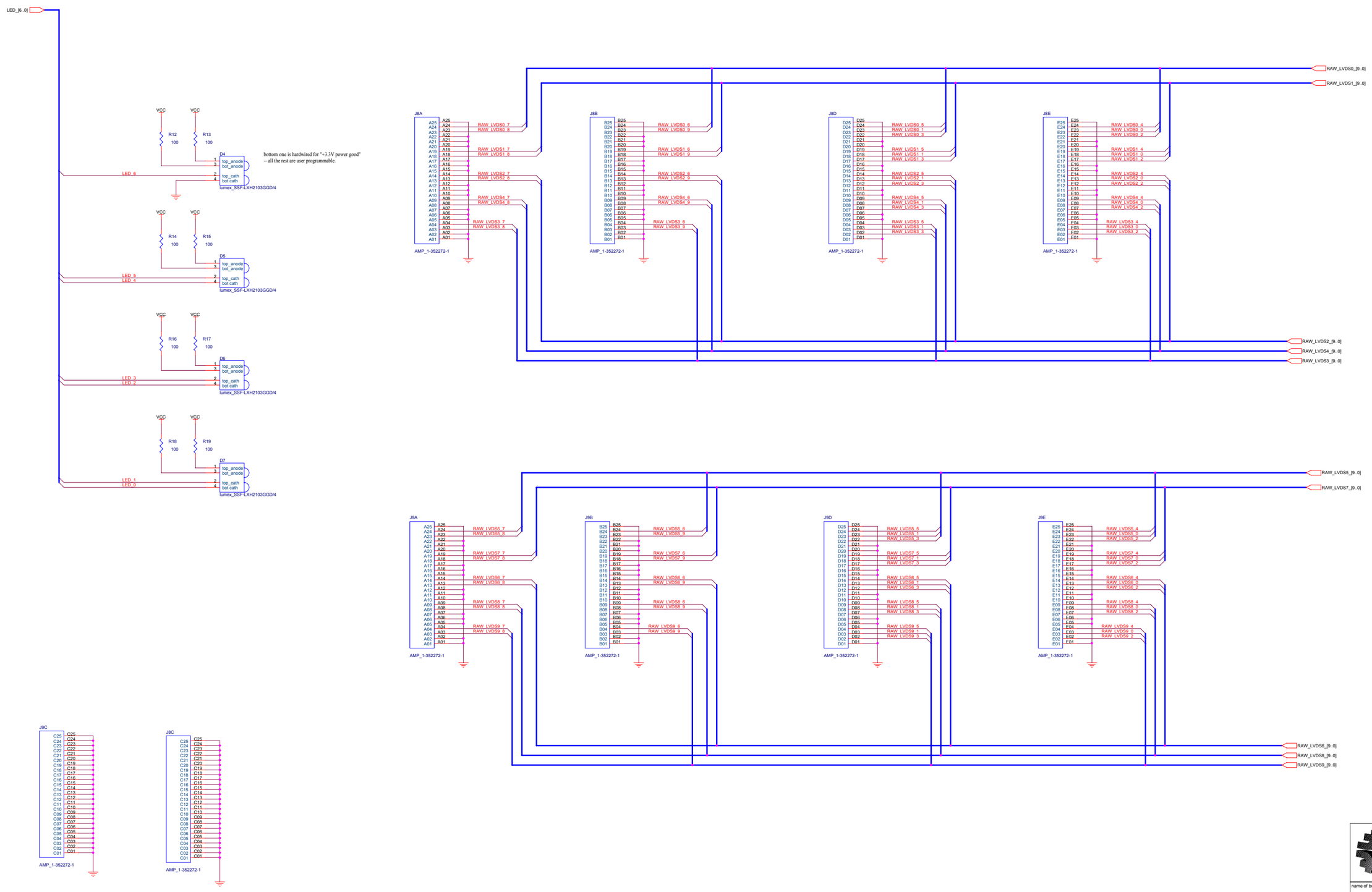


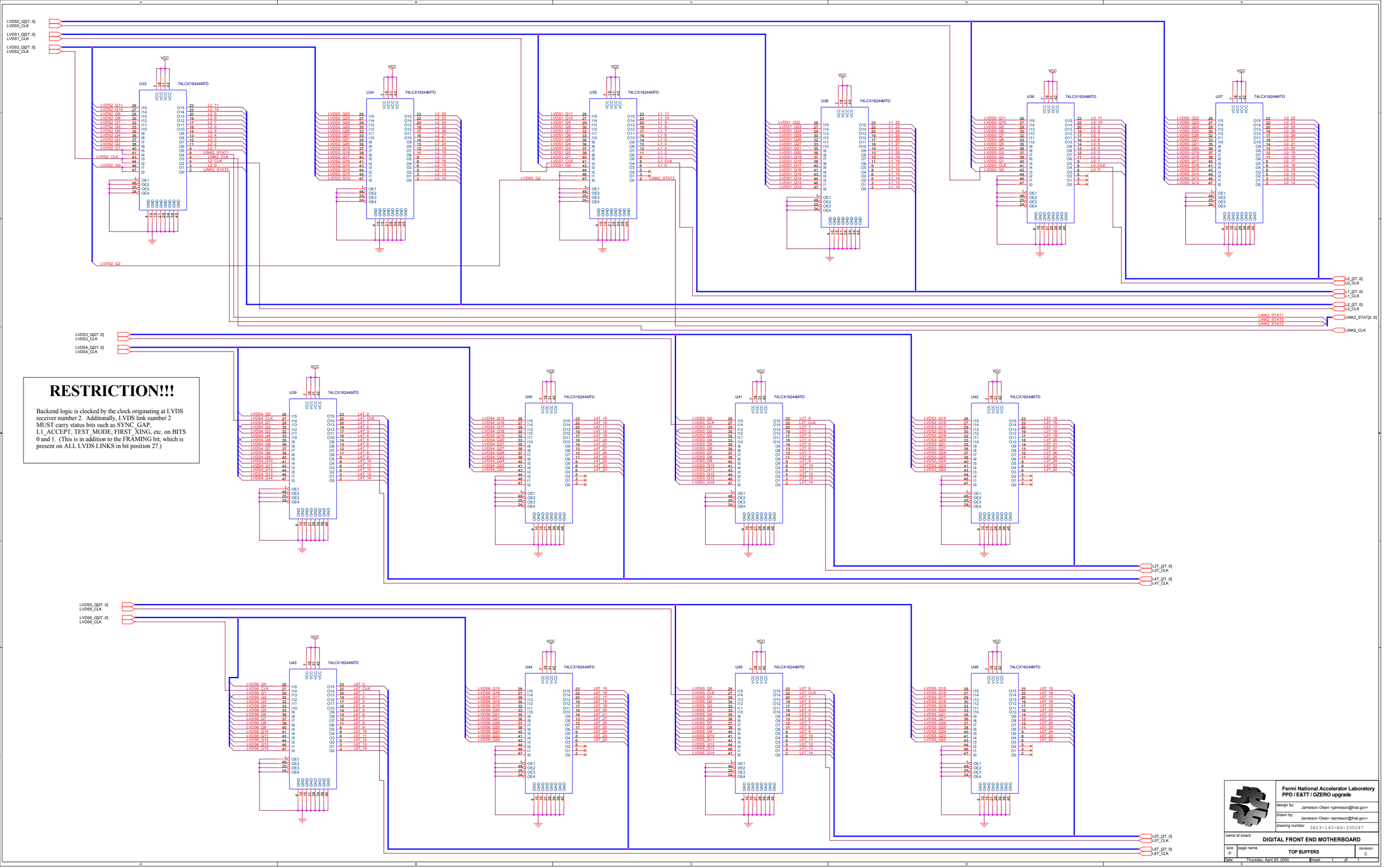
Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-140-ED-330247

name of board: **DIGITAL FRONT END MOTHERBOARD**

size	page name	revision
D	**FRONT PANEL**	C

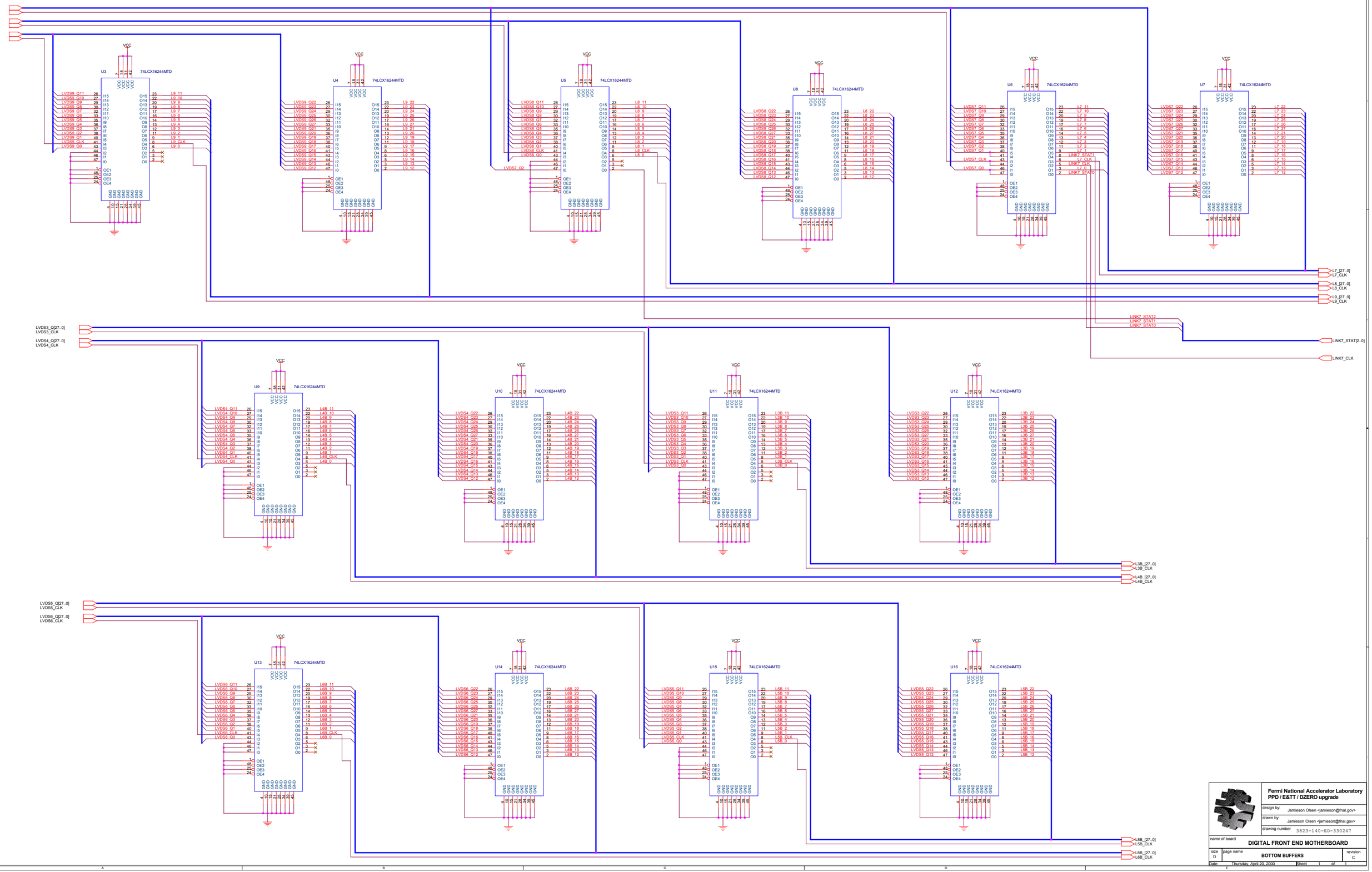
Date: Thursday, April 20, 2000 Sheet 1 of 1



RESTRICTION!!!

Backend logic is clocked by the clock originating at LVDS receiver number 2. Additonally, LVDS link number 2 MUST carry status bits such as SYNC_GAP, L1_ACCEPT, TEST_MODE, FIRST_XING, etc. on BITS 0 and 1. (This is in addition to the FRAMING bit, which is present on ALL LVDS LINKS in bit position 27.)

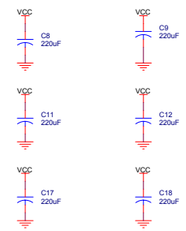
Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade	
design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-140-ED-330247
name of board	DIGITAL FRONT END MOTHERBOARD
size D	page name TOP BUFFERS
revision C	
date: Thursday, April 20, 2000	Sheet 1 of 1



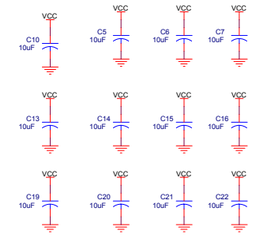
Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

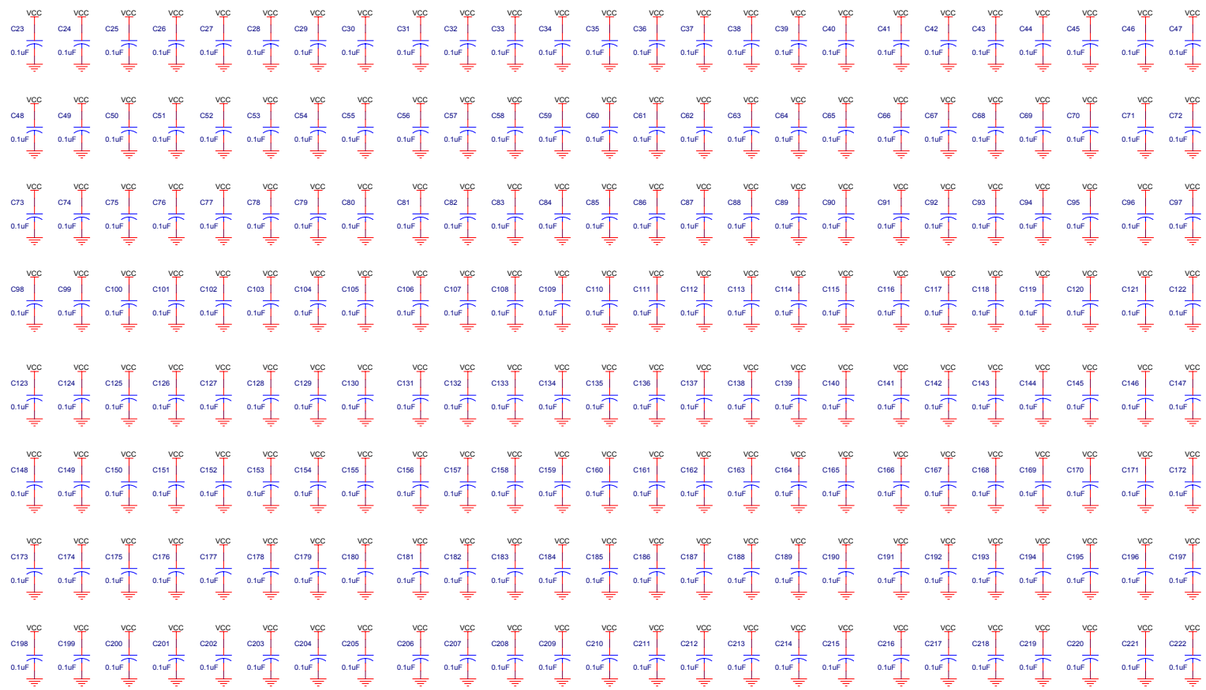
design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-140-ED-330247
name of board	DIGITAL FRONT END MOTHERBOARD
size	D
page name	BOTTOM BUFFERS
revision	C
date:	Thursday, April 20, 2000
Sheet	1 of 1

USE PANASONIC V0GA221P SMALL CAN SMT DEVICES HERE (DIGIKEY)



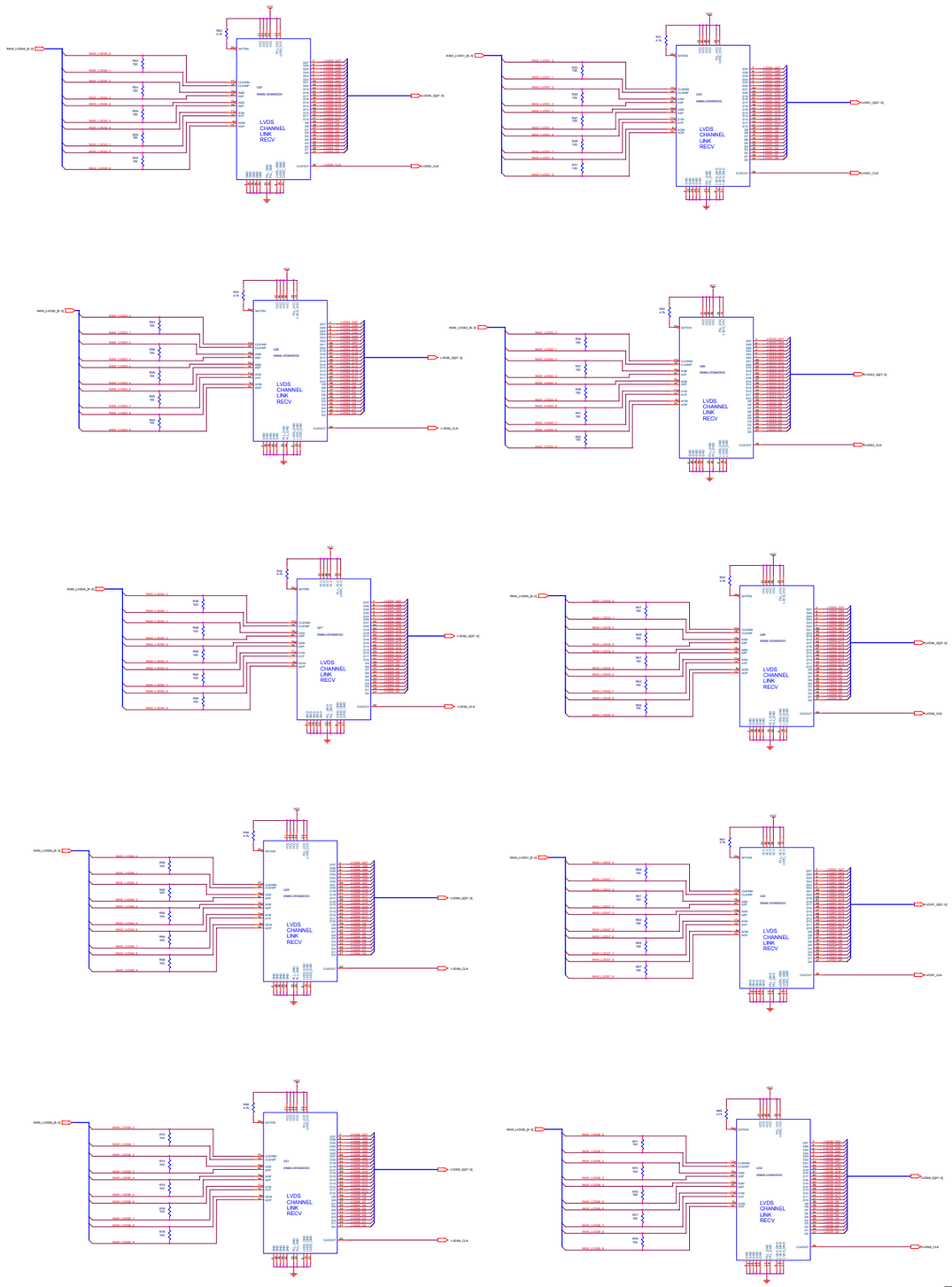
USE PANASONIC ECS-T0JY106R SMT DEVICES HERE. FOOTPRINT IS STANDARD 3216 STYLE. (DIGIKEY)





FOR THESE JUST USE 0805 .1 uF CAPS, NPO, X7R, ETC.

Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade	
design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-140-ED-330247
name of board	DIGITAL FRONT END MOTHERBOARD
size D / page name	BYPASS CAPS / revision C
Date: Thursday, April 20, 2000	Sheet 1 of 1



Fermi National Accelerator Laboratory
PPD / ESE/TT /GEDRC/upgrade

author/s: Jeremias Diaz< cjeremias@fnal.gov>
drawn by: Jeremias Diaz< cjeremias@fnal.gov>
drawing number: 2562-2-1-0-B0-1-01010-A-R

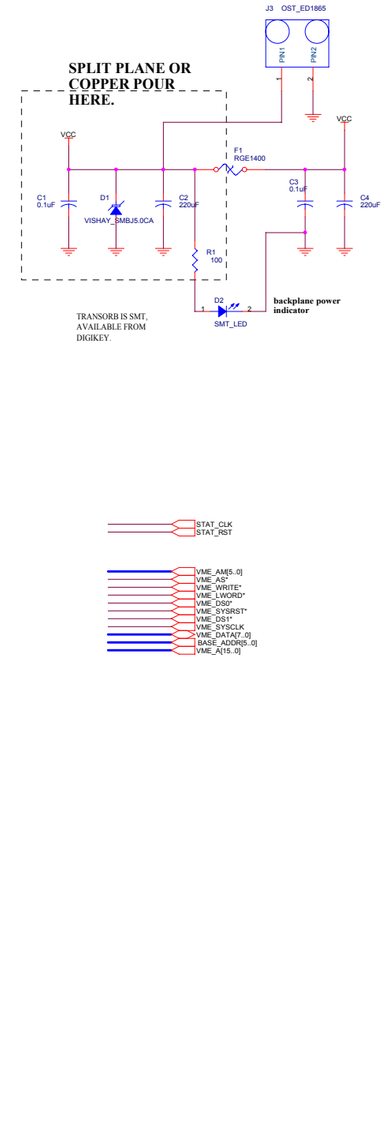
DIGITAL FRONT END MOTHERBOARD

LVDS CHANNEL LINK RECEIVERS

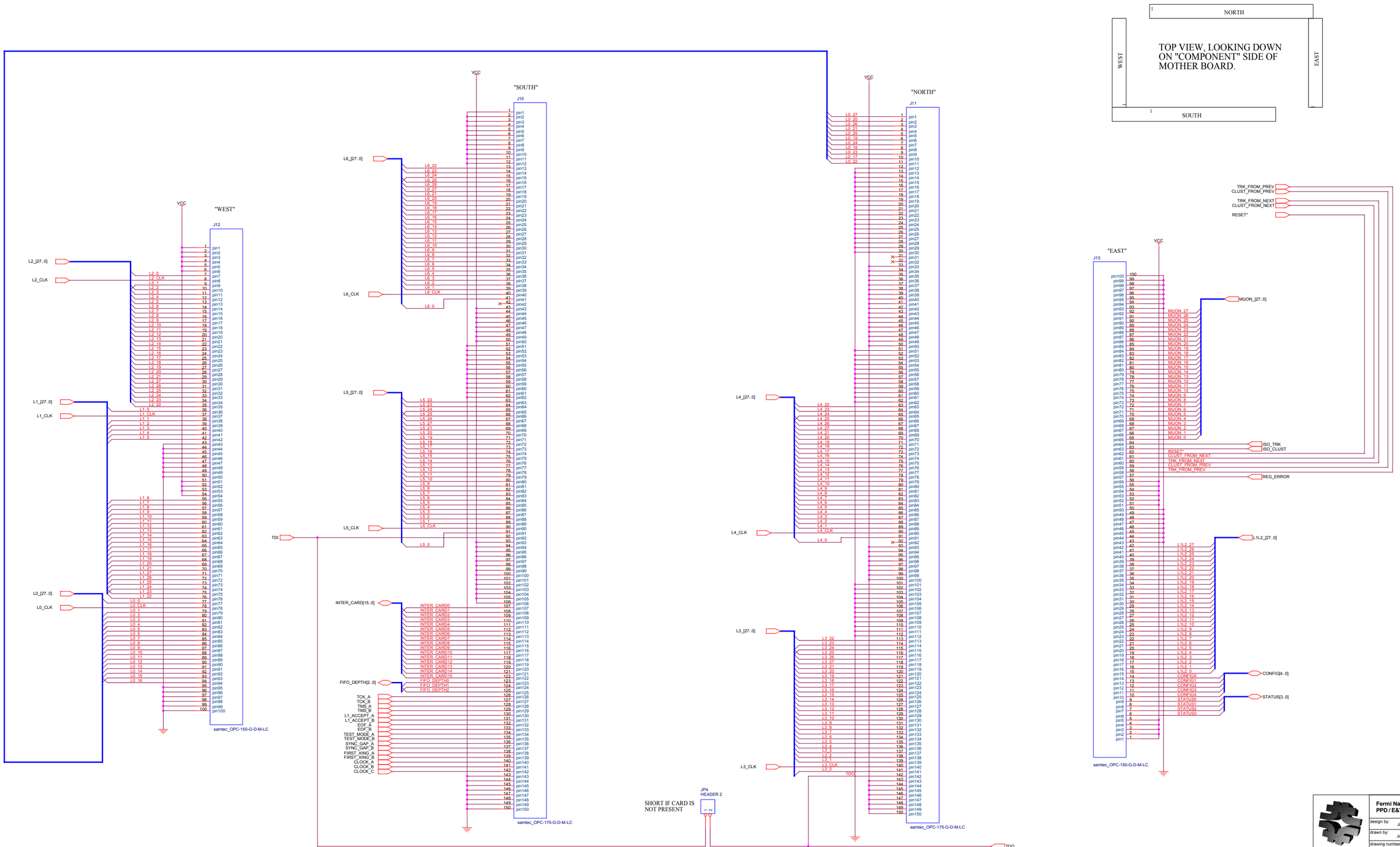
sheet 1 of 1 board: 1 of 1 | size: A3 | date: 2022-Jun-06 | revision: 1.0

HORIZONTAL TERMINAL BLOCK FOR BENCH TESTING. POSITION NEAR THE BACK OF THE BOARD, POINTING TOWARDS THE EDGE OF THE BOARD. ON-SHORE TECH MODEL ED1865. REQUIRES A SECOND PIECE, MODEL ED1773.

PANASONIC METAL CAN CAP, AVAILABLE FROM DIGIKEY. 220uF NOTE CASE OUTLINE IS LARGER THAN FOOTPRINT...



Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade	
design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-140-ED-330247
name of board	DIGITAL FRONT END MOTHERBOARD
size D / page name	BACKPLANE CONNECTION / revision C
date:	Thursday, April 20, 2000
Sheet	1 of 1



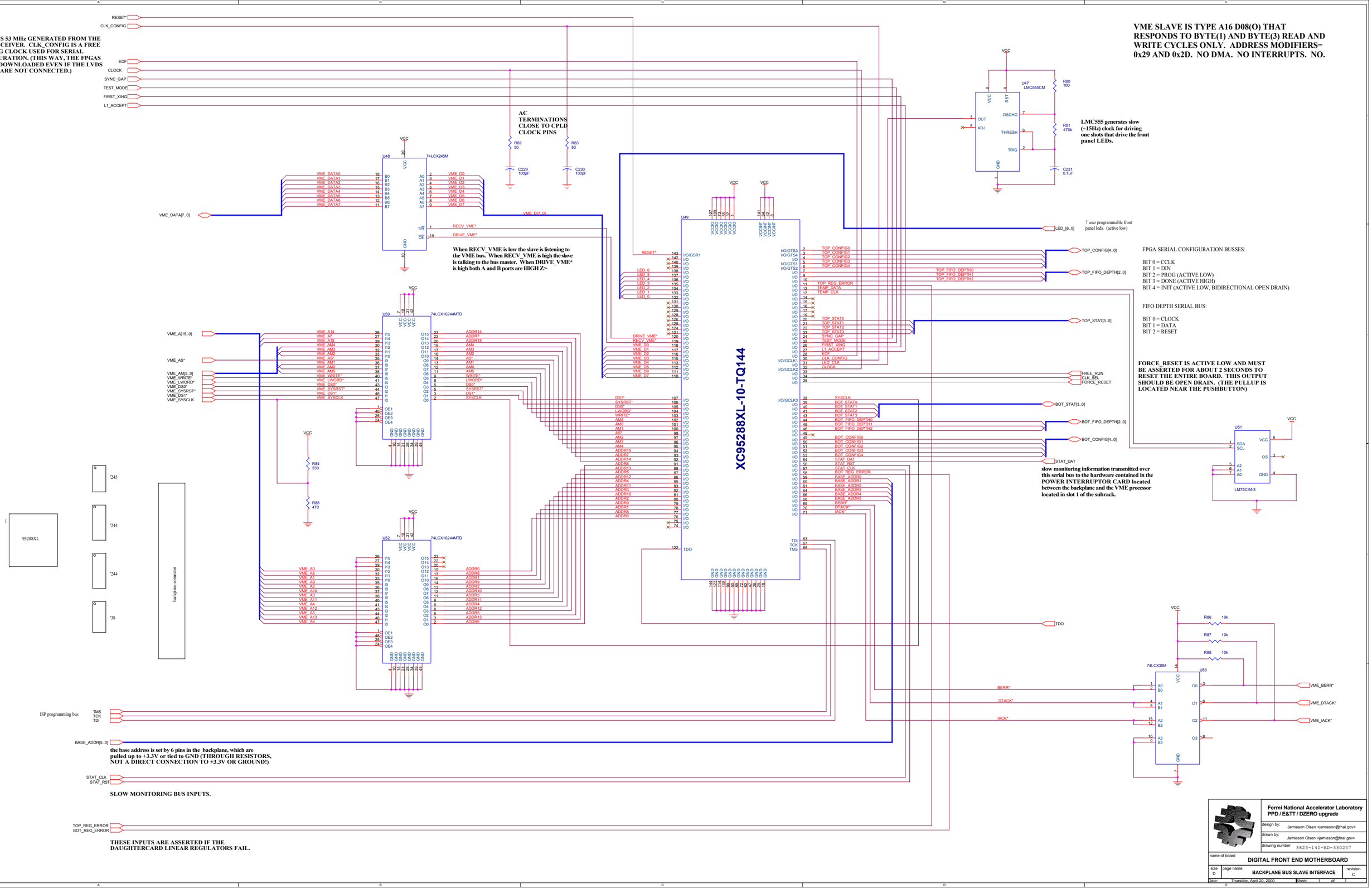
Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

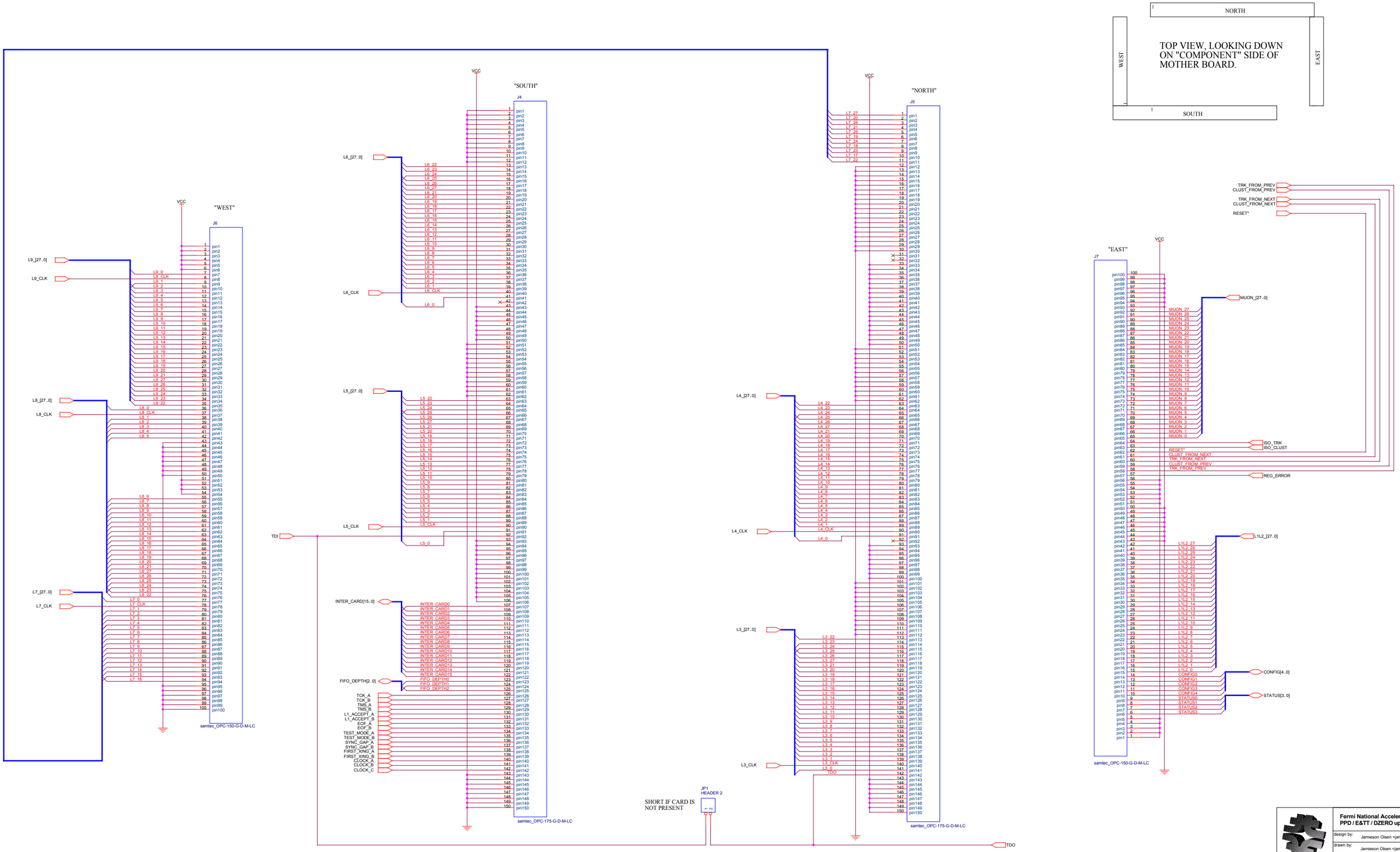
design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-140-ED-330247

name of board: **DIGITAL FRONT END MOTHERBOARD**

size	page name	revision
D	TOP DAUGHTERBOARD CONNECTION	C

Date: Thursday, April 20, 2000 Sheet 1 of 1


CLOCK IS 53 MHz GENERATED FROM THE LVDS RECEIVER. CLK_CONFIG IS A FREE RUNNING CLOCK USED FOR SERIAL CONFIGURATION. (THIS WAY, THE FPGAS CAN BE DOWNLOADED EVEN IF THE LVDS CABLES ARE NOT CONNECTED.)
VME SLAVE IS TYPE A16 D08(O) THAT RESPONDS TO BYTE(1) AND BYTE(3) READ AND WRITE CYCLES ONLY. ADDRESS MODIFIERS= 0x29 AND 0x2D. NO DMA. NO INTERRUPTS. NO.
AC TERMINATIONS CLOSE TO CPLD CLOCK PINS
When RECV_VME is low the slave is listening to the VME bus. When RECV_VME is high the slave is talking to the bus master. When DRIVE_VME* is high both A and B ports are HIGH Z>
LMC555 generates slow (~15Hz) clock for driving one shots that drive the front panel LEDs.
7 user programmable front panel leds. (active low)
FPGA SERIAL CONFIGURATION BUSSES:
BIT 0 = CCLK
BIT 1 = DIN
BIT 2 = PROG (ACTIVE LOW)
BIT 3 = DONE (ACTIVE HIGH)
BIT 4 = INIT (ACTIVE LOW, BIDIRECTIONAL OPEN DRAIN)
FIFO DEPTH SERIAL BUS:
BIT 0 = CLOCK
BIT 1 = DATA
BIT 2 = RESET
FORCE_RESET IS ACTIVE LOW AND MUST BE ASSERTED FOR ABOUT 2 SECONDS TO RESET THE ENTIRE BOARD. THIS OUTPUT SHOULD BE OPEN DRAIN. (THE PULLUP IS LOCATED NEAR THE PUSHBUTTON)
slow monitoring information transmitted over this serial bus to the hardware contained in the POWER INTERRUPTOR CARD located between the backplane and the VME processor located in slot 1 of the subrack.
the base address is set by 6 pins in the backplane, which are pulled up to +3.3V or tied to GND (THROUGH RESISTORS, NOT A DIRECT CONNECTION TO +3.3V OR GROUND!)
SLOW MONITORING BUS INPUTS.
THESE INPUTS ARE ASSERTED IF THE DAUGHTERCARD LINEAR REGULATORS FAIL.
XC95288XL-10-TQ144
74LCX245M
74LCX16244MTD
LM555CM
LM75CIM-3
74LCX38M
95288XL
'245
'244
'244
'38
backplane connector
ISP programming bus
Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade
design by: Jamieson Olsen <jamieson@fnal.gov>
drawn by: Jamieson Olsen <jamieson@fnal.gov>
drawing number 3823-140-ED-330247
name of board
DIGITAL FRONT END MOTHERBOARD
size D
page name
BACKPLANE BUS SLAVE INTERFACE
revision C
Date: Thursday, April 20, 2000
Sheet 1 of 1



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PPD / E&TT / DZERO upgrade

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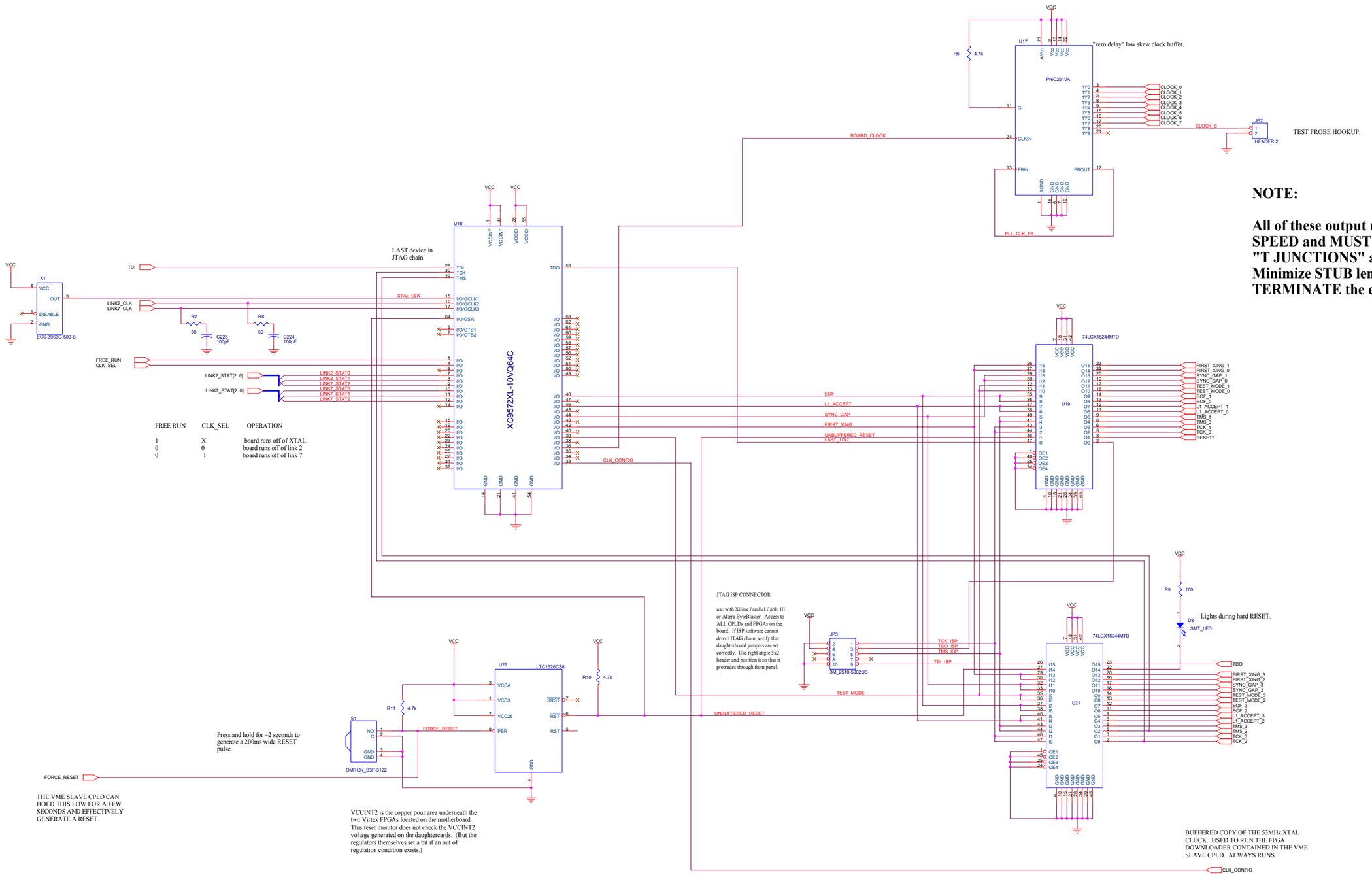
name of board	DIGITAL FRONT END MOTHERBOARD
size	D
page name	BOTTOM DAUGHTERBOARD CONNECTION
revision	C
Date:	Thursday, April 20, 2000
Sheet	1 of 1



FREE RUN	CLK_SEL	OPERATION
1	X	board runs off of XTAL
0	0	board runs off of link 2
0	1	board runs off of link 7

NOTE:

All of these output nets are HIGH SPEED and MUST be routed without "T JUNCTIONS" and BRANCHES. Minimize STUB length and AC TERMINATE the end of the trace.

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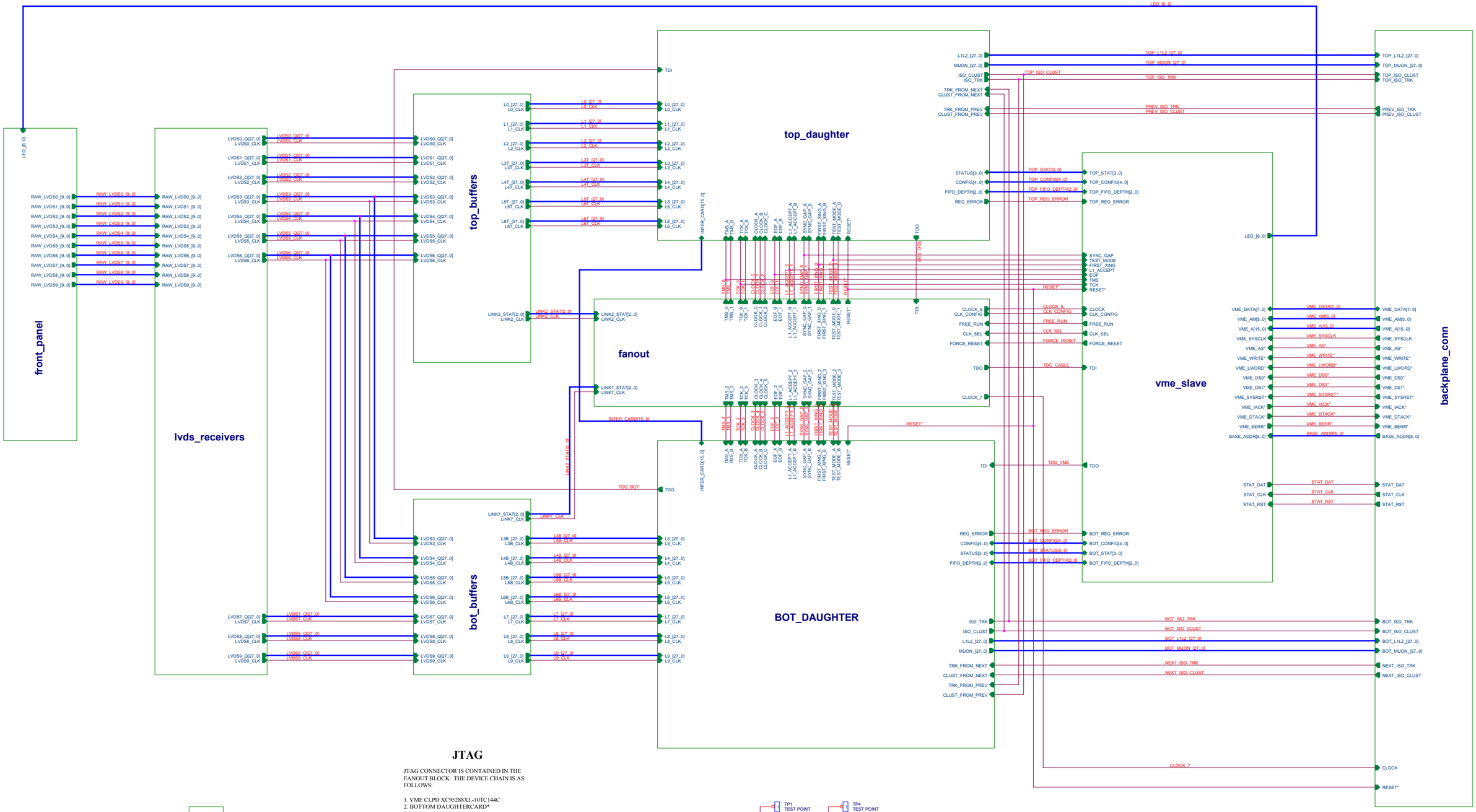
drawing number	3823-140-ED-330247
name of board	DIGITAL FRONT END MOTHERBOARD
size D	page name: TIMING and CONTROL SIGNAL FANOUT
revision C	
Date: Thursday, April 20, 2000	Sheet 1 of 1

DIGITAL FRONT END MOTHERBOARD TOP LEVEL



JTAG

JTAG CONNECTOR IS CONTAINED IN THE FANOUT BLOCK. THE DEVICE CHAIN IS AS FOLLOWS:

1. VME CLPD XC95288XL-10TC144C
2. BOTTOM DAUGHTERCARD*
3. TOP DAUGHTERCARD*
4. TIMING CPLD XC9572XL-10VQ64C

* DAUGHTERCARDS CAN BE BYPASSED WITH A JUMPER ON THE MOTHERBOARD. UP TO 8 JTAG DEVICES ARE SUPPORTED ON EACH OF THE DAUGHTERCARDS.

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drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-140-ED-330247
name of board	DIGITAL FRONT END MOTHERBOARD
size D	page name TOP LEVEL
revision C	
date: Tuesday, December 04, 2001	Sheet 1 of 1