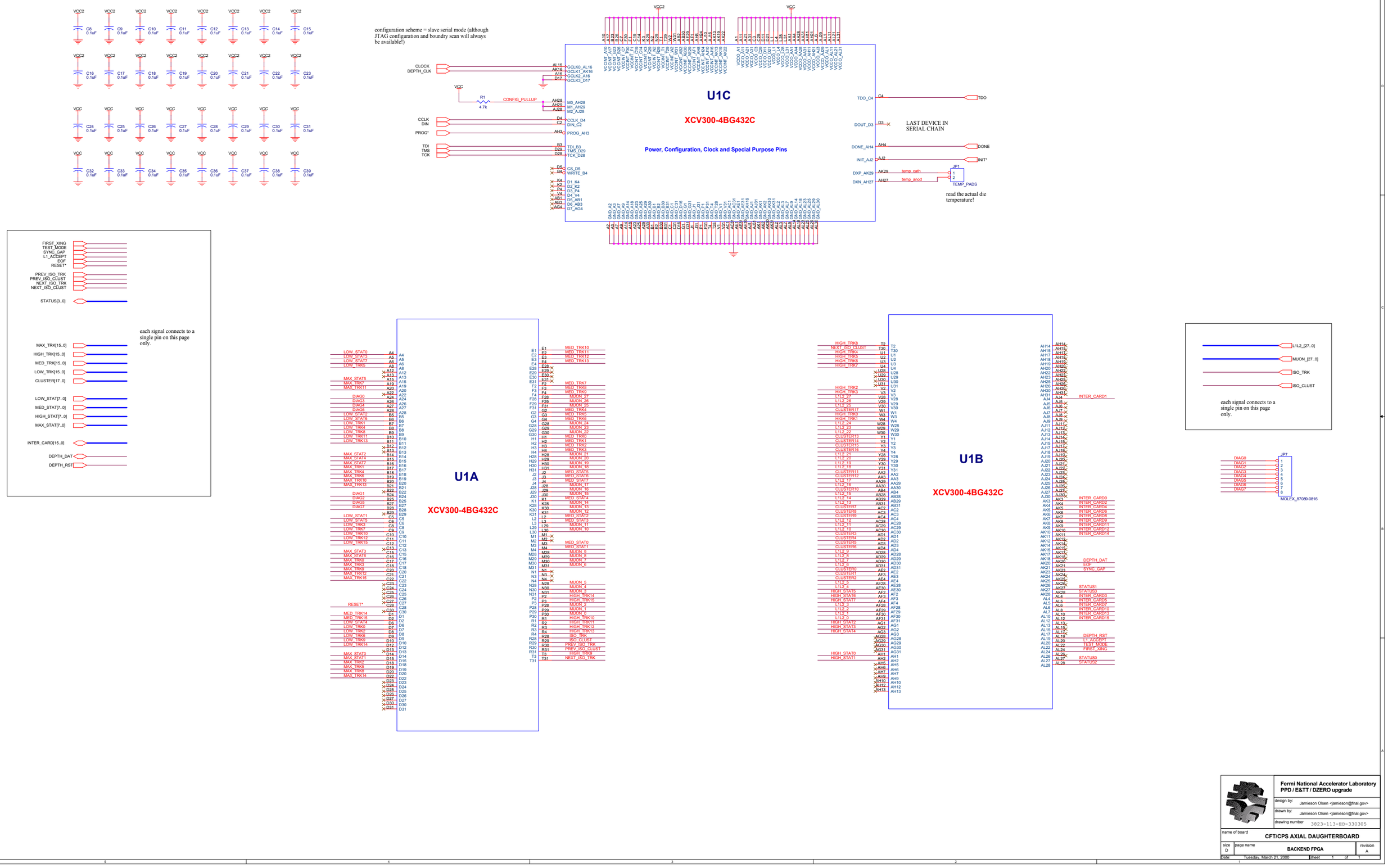
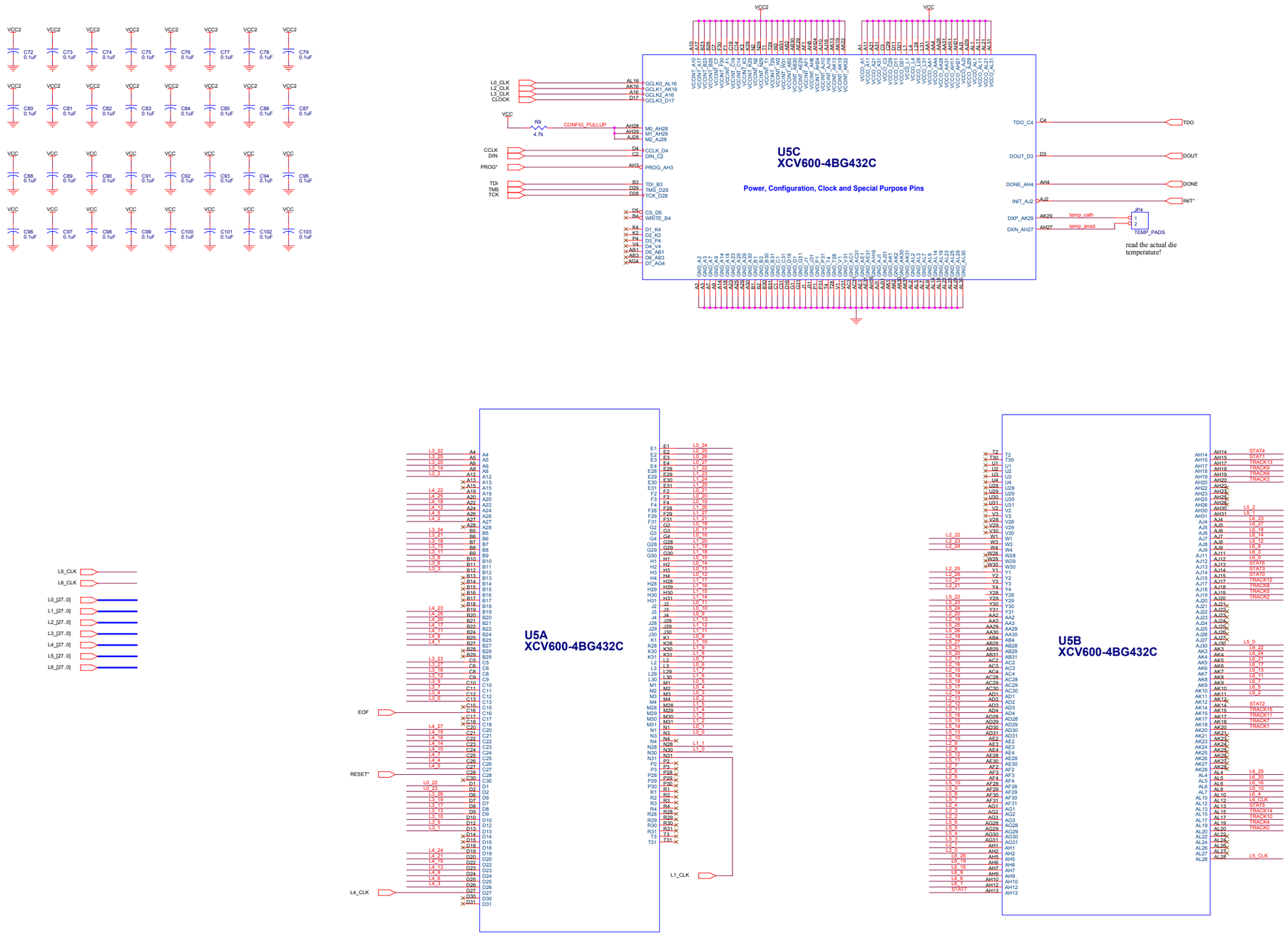


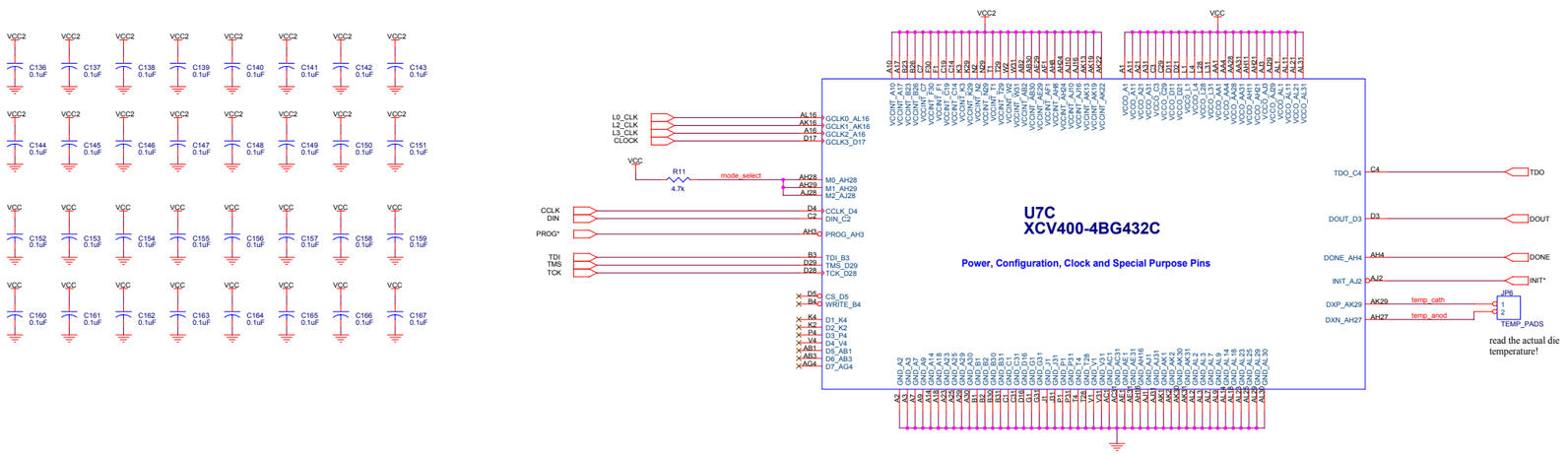
Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

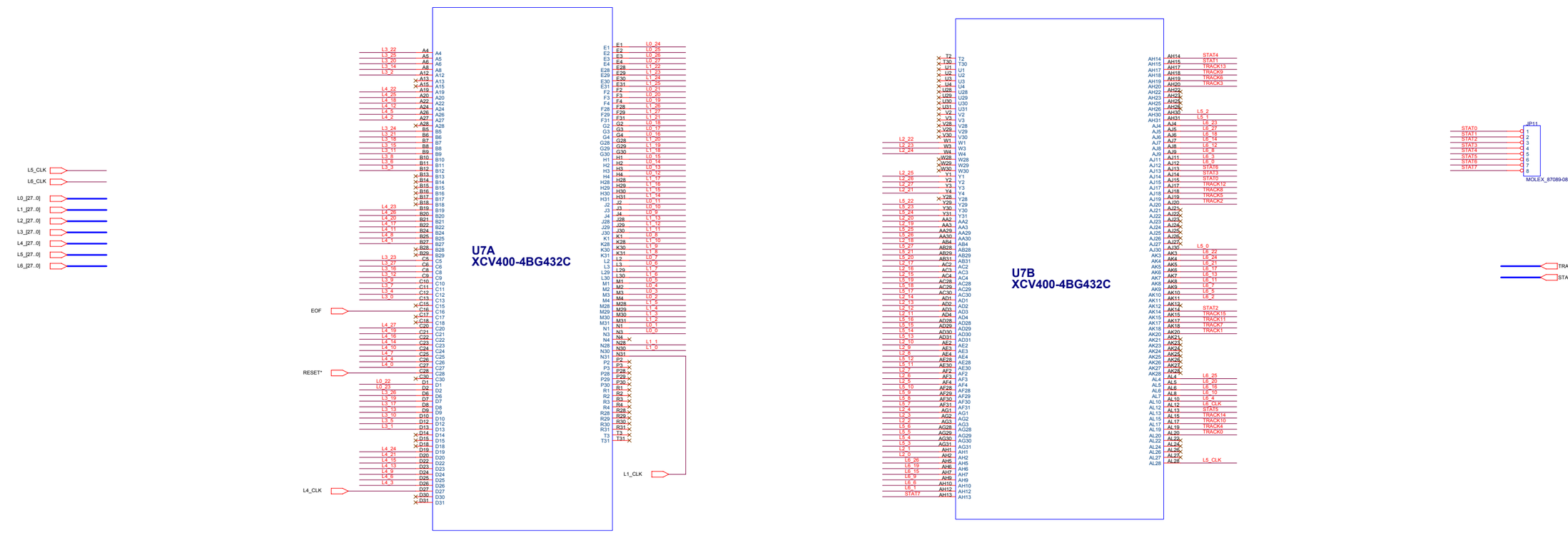
design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-113-ED-330305
name of board	CFT/CPS AXIAL DAUGHTERBOARD
size D	page name BACKEND FPGA
revision A	
Date:	Tuesday, March 21, 2000
Sheet	1 of 1



Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

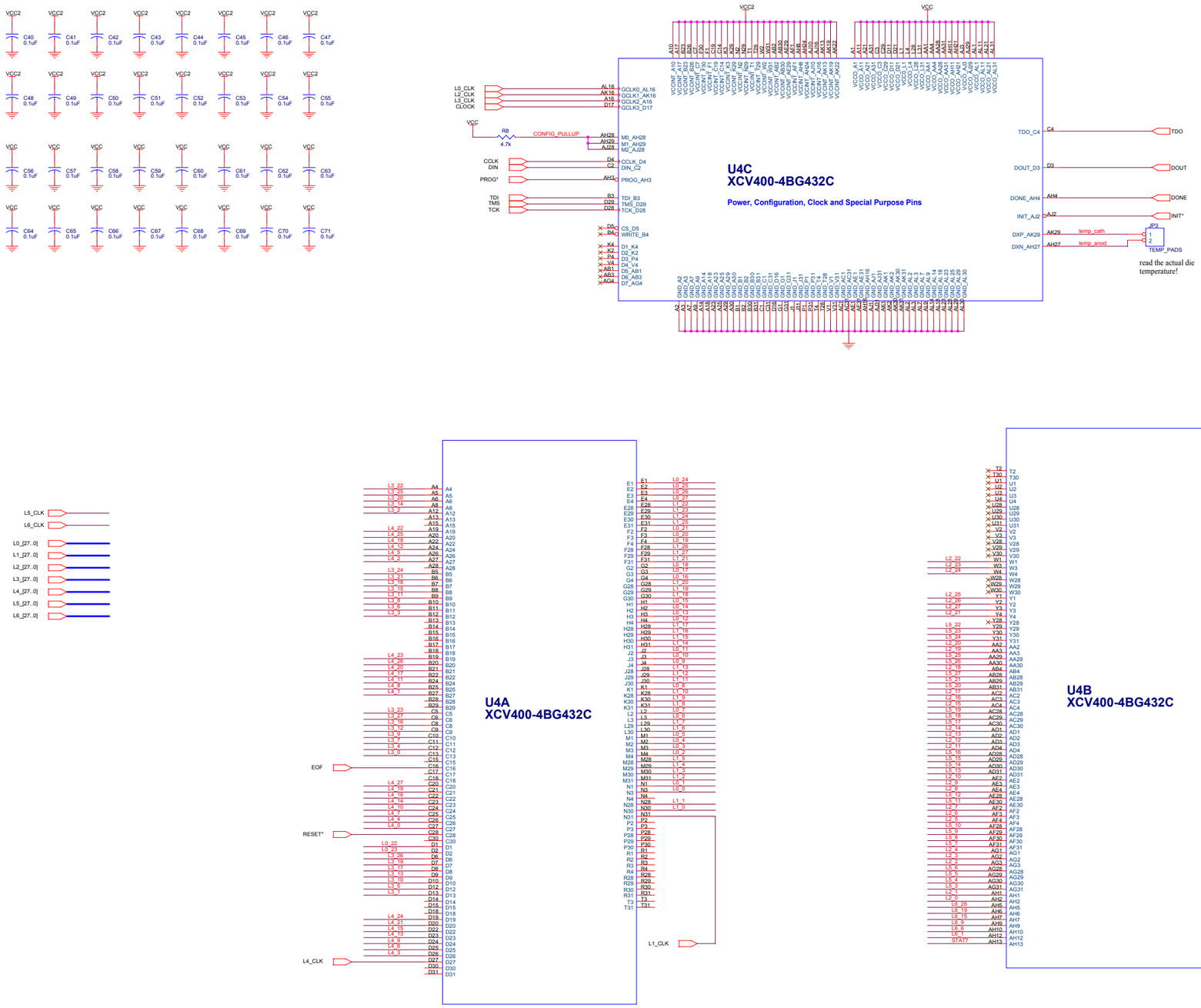
design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-113-ED-330305
name of board	CFT/CPS AXIAL DAUGHTERBOARD
size D	page name: LOWEST Pt TRACK FINDER FPGA
revision A	
Date: Tuesday, March 21, 2000	Sheet 1 of 1





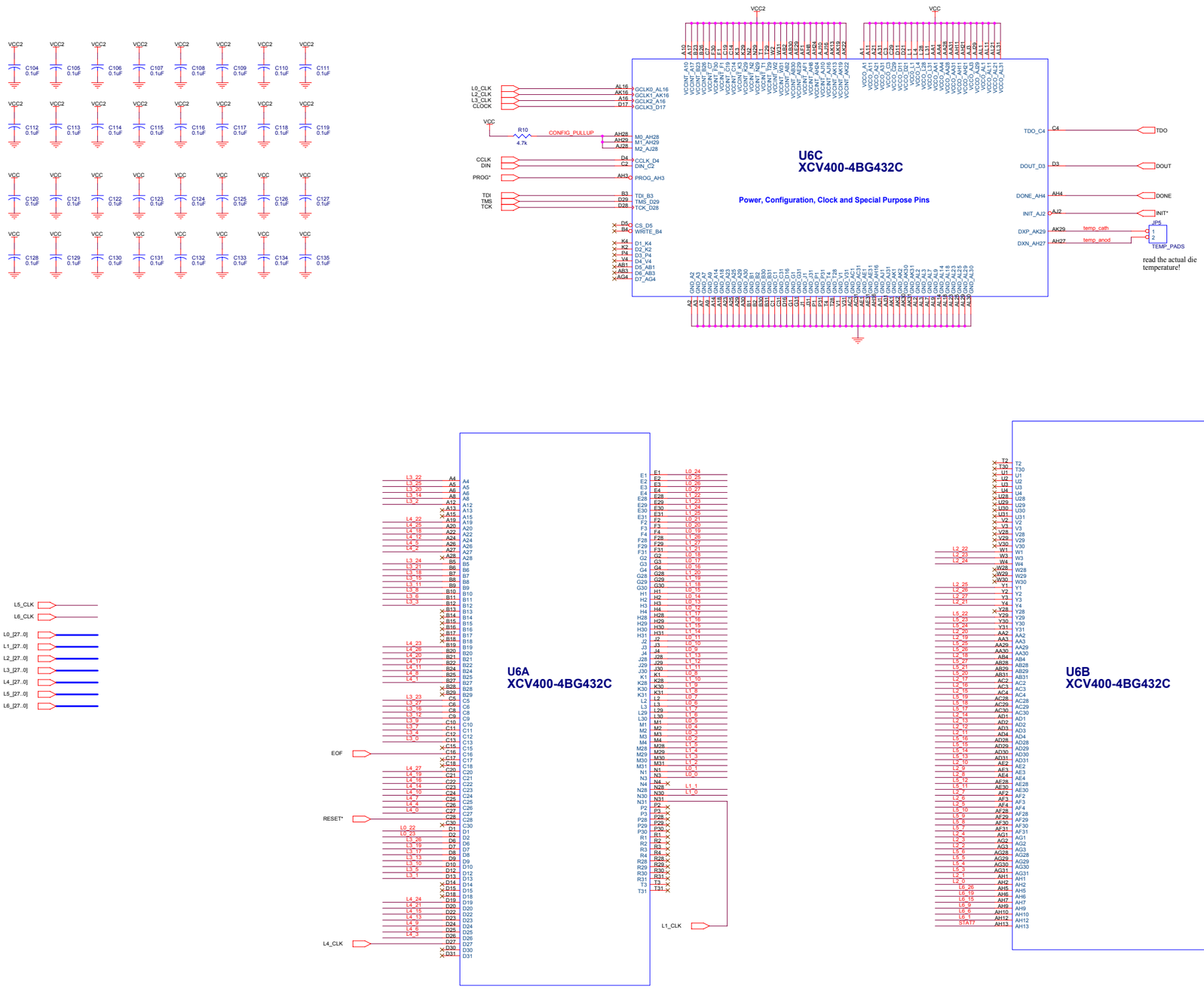
Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-113-ED-330305
name of board	CFT/CPS AXIAL DAUGHTERBOARD
size D	page name: MEDIUM Pt TRACK FINDER FPGA
revision	A
Date:	Tuesday, March 21, 2000
Sheet	1 of 1



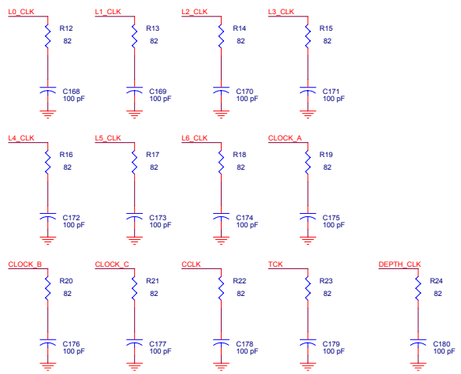
Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-113-ED-330305
name of board	CFT/CPS AXIAL DAUGHTERBOARD
size D	page name HIGH Pt TRACK FINDER FPGA
revision	A
Date:	Tuesday, March 21, 2000
Sheet	1 of 1

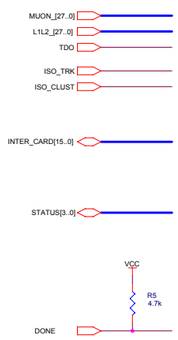


Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-113-ED-330305
name of board	CFT/CPS AXIAL DAUGHTERBOARD
size D	page name: MAXIMUM Pt TRACK FINDER FPGA
revision	A
Date:	Tuesday, March 21, 2000
Sheet	1 of 1

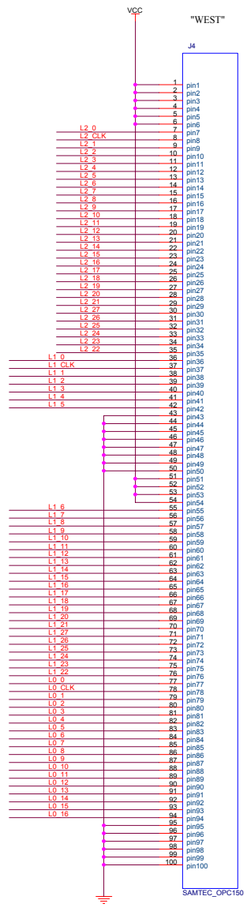


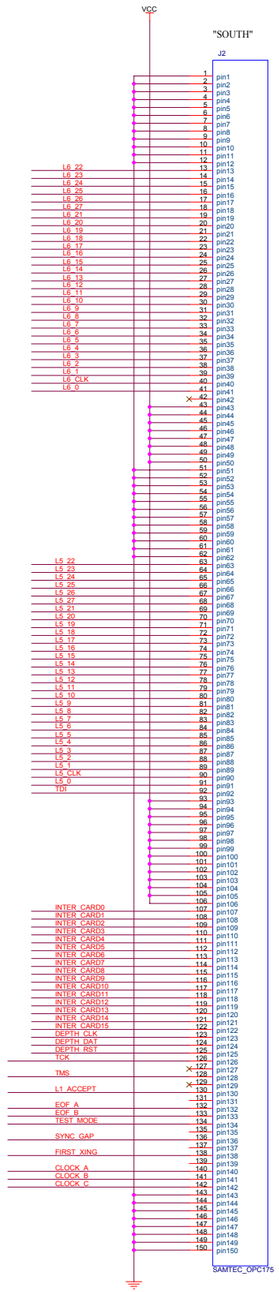
Although shown here as inputs, these nets are actually outputs from the daughterboard. i.e. the daughtercard drives these nets.

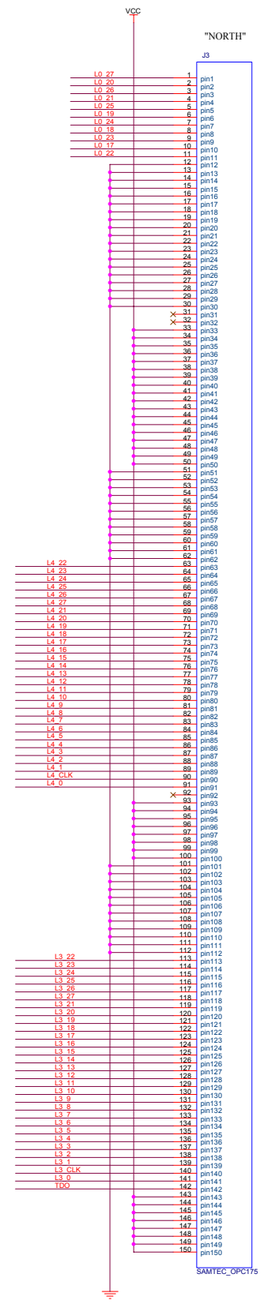


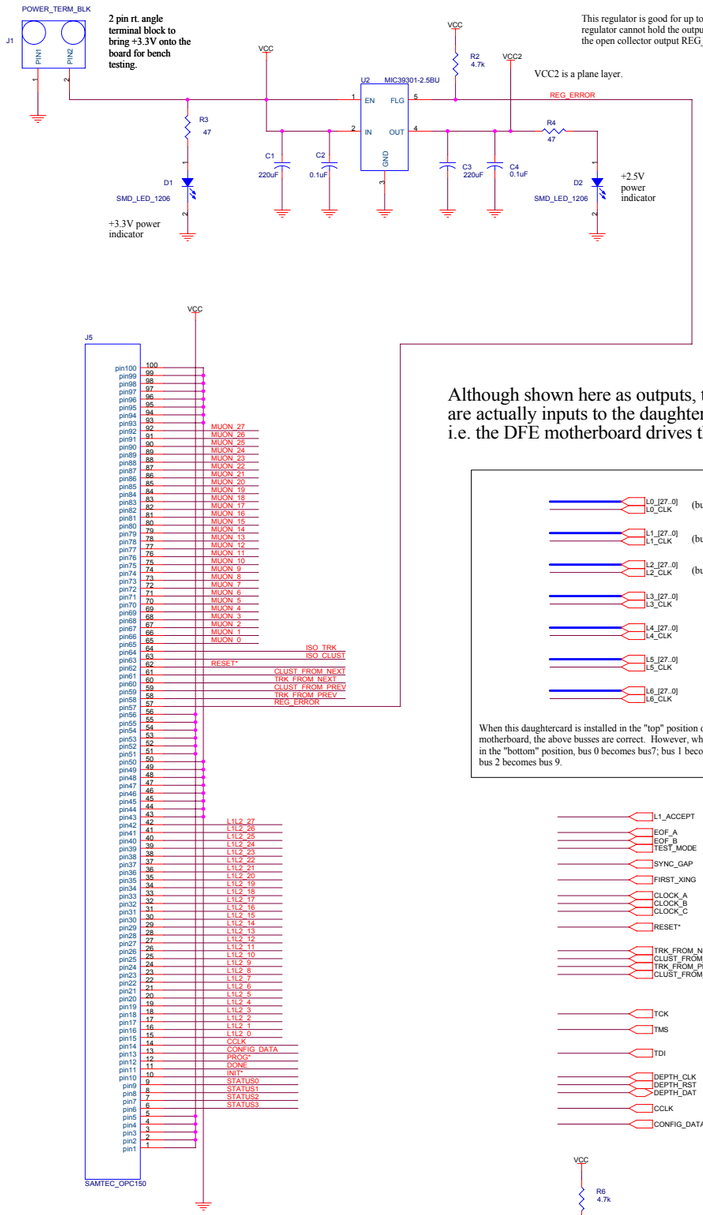
DONE goes high after all of the FPGAs have been configured.

Implict connections on this page only. With the exception of power and ground, each net on this page terminates or originates at a single pin.



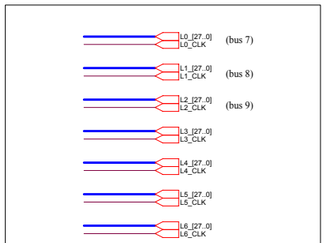




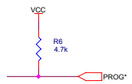


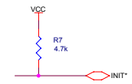
This regulator is good for up to 3A @ 2.5V. If the regulator cannot hold the output to 2.5V, it will pull the open collector output REG_ERROR low.

Although shown here as outputs, these nets are actually inputs to the daughterboard. i.e. the DFE motherboard drives these nets.

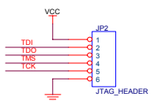


When this daughtercard is installed in the "top" position on the DFE motherboard, the above busses are correct. However, when it is installed in the "bottom" position, bus 0 becomes bus7; bus 1 becomes bus 8; and bus 2 becomes bus 9.

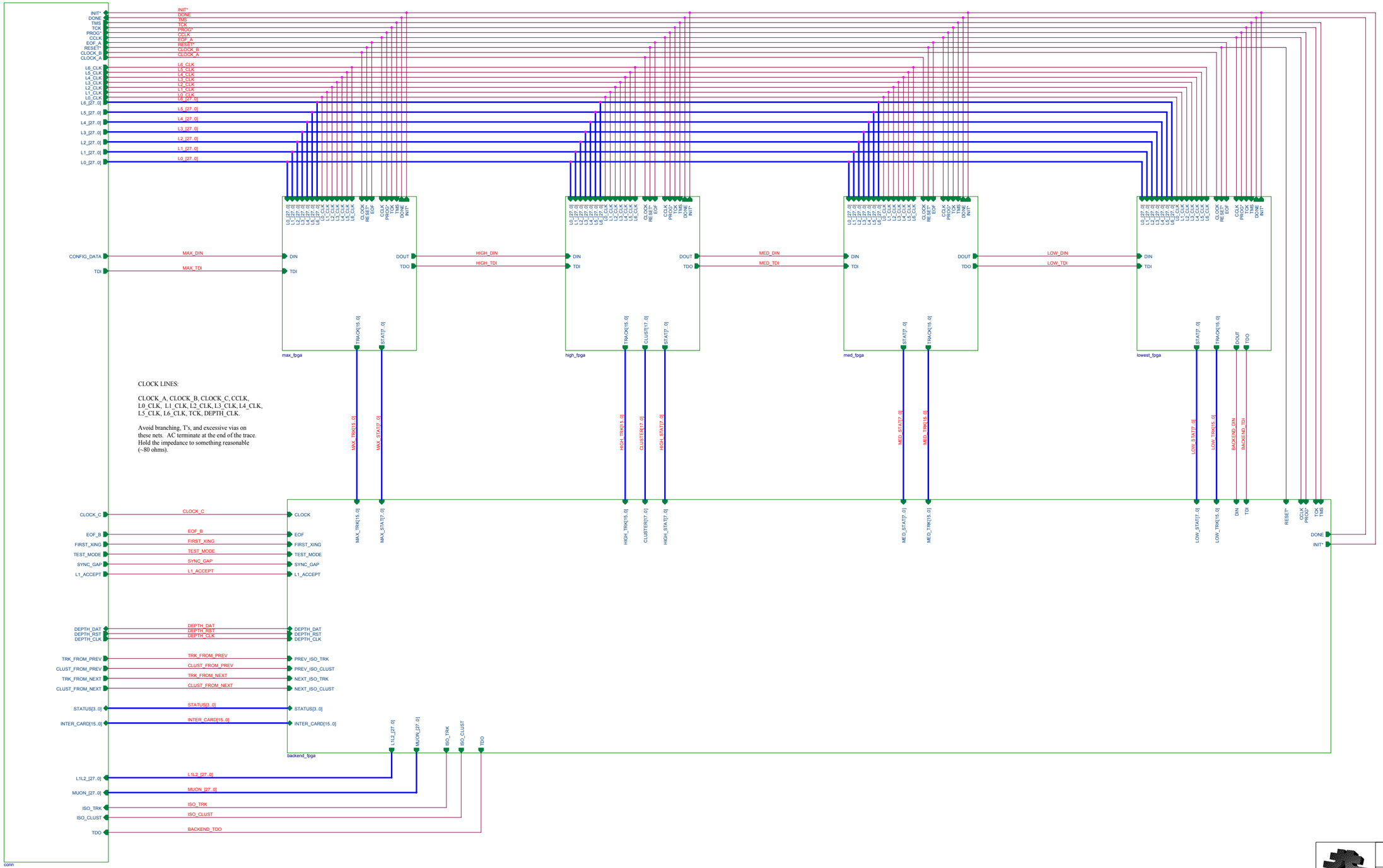




active-low, open-drain fpga configuration signals.



Fermi National Accelerator Laboratory PPD / E&TT / DZERO upgrade	
design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-113-ED-330305
name of board	CFT/CPS AXIAL DAUGHTERBOARD
size D	page name CONNECTION TO MOTHERBOARD
revision A	
Date: Tuesday, March 21, 2000	Sheet 1 of 1



Fermi National Accelerator Laboratory
PPD / E&TT / DZERO upgrade

design by:	Jamieson Olsen <jamieson@fnal.gov>
drawn by:	Jamieson Olsen <jamieson@fnal.gov>
drawing number	3823-113-ED-330305
name of board	**CFT/CPS AXIAL DAUGHTERBOARD**
size D	page name **TOP LEVEL**
revision A	
Date:	Tuesday, March 21, 2000
Sheet	1 of 1